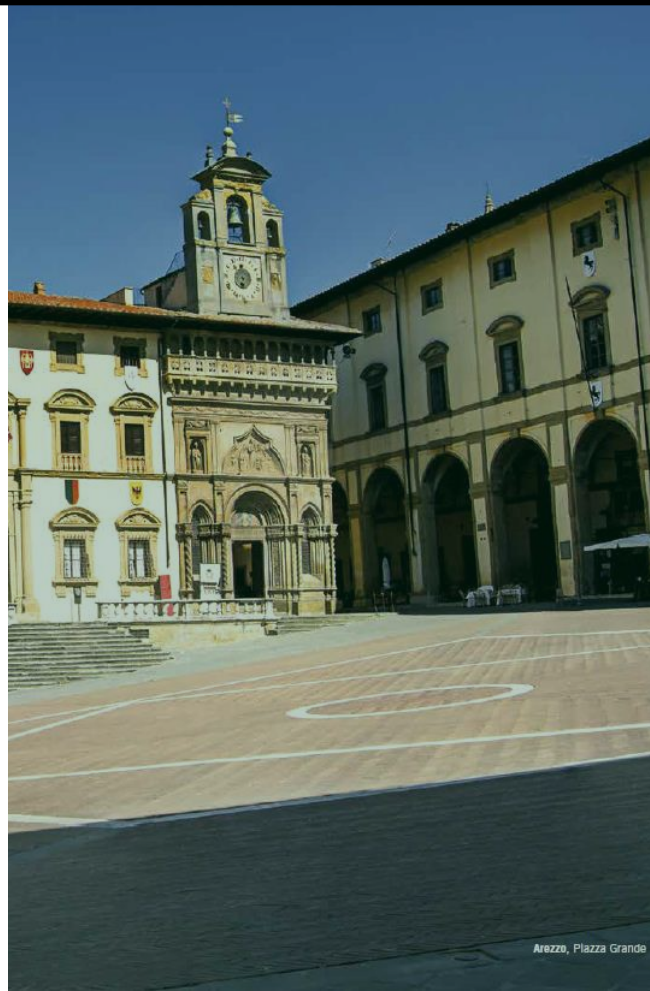
How the history began

Two friends with
a passion for electronics
in a garage of Arezzo

SECO GROUP

EMBEDDED CREATORS
SINCE 1979



SECO today

Today SECO is a world-leader in **electronic embedded** solutions, providing innovative, **high quality**, reliable solutions for **all embedded sectors** and makers.

With highly **experienced engineers** and hi-tech equipment, SECO **designs** and **manufactures** all-in-house **in Italy** state-of-the-art **standard** products and **custom** solutions.

SECO at a glance

Branch offices

HQ: Arezzo (Italy)
Milan (Italy)

Boston
(USA)

Bangalore
(India)

Taipei
(Taiwan)

Frankfurt
(Germany)

Turnover:

€ 47+ mil.
in 2016

Human resources:

234 people
at 04.14.2017

Why are we here today?

INDUSTRY

ACADEMY

Specialistic Technologies

Multidisciplinarity

Networking

Different Markets

AXIOM Ecosystem

H2020 allowed SECO to invest in the **Programmable hybrid ARM/FPGA SoCs** area bringing **new solutions** to the embedded market through relationships with both **industrial and academic partners**

INDUSTRIAL PARTNERS

SECO

herta security

VIMAR energia positiva

EVIDENCE EMBEDDING TECHNOLOGY

ACADEMIC PARTNERS

BSC Barcelona Supercomputing Center Centro Nacional de Supercomputación

UNIVERSITATIS SEMARUM MCCXXXX

UPC

FORTH Institute of Computer Science

Background Scenario: The Market Needs

CYBER-PHYSICAL AGE

Internet of Things

Machine Learning

Predicting Models

Things have to become **as smart as people**

in order to improve and **simplify human behavior**

Our proposal: AXIOM

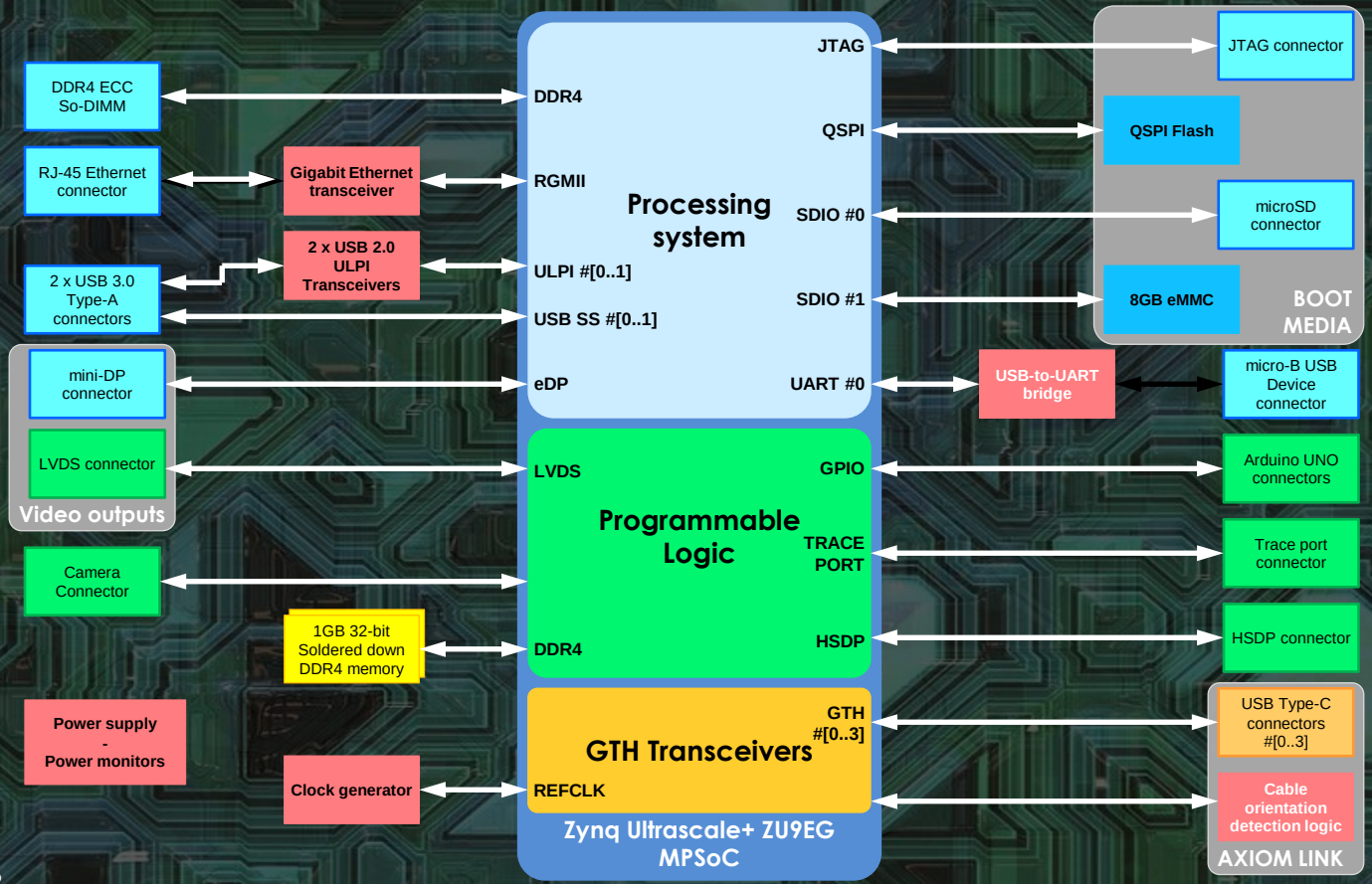
- Hybrid SoC
- ARM based
- Compatibility with Arduino
- Cost-effective networing infrastructure
- Open source OS
- OmpSs framework
- Clustering capabilities

Hardware

Software

Hardware and **Software Stack Solution**

AXIOM hardware prototype



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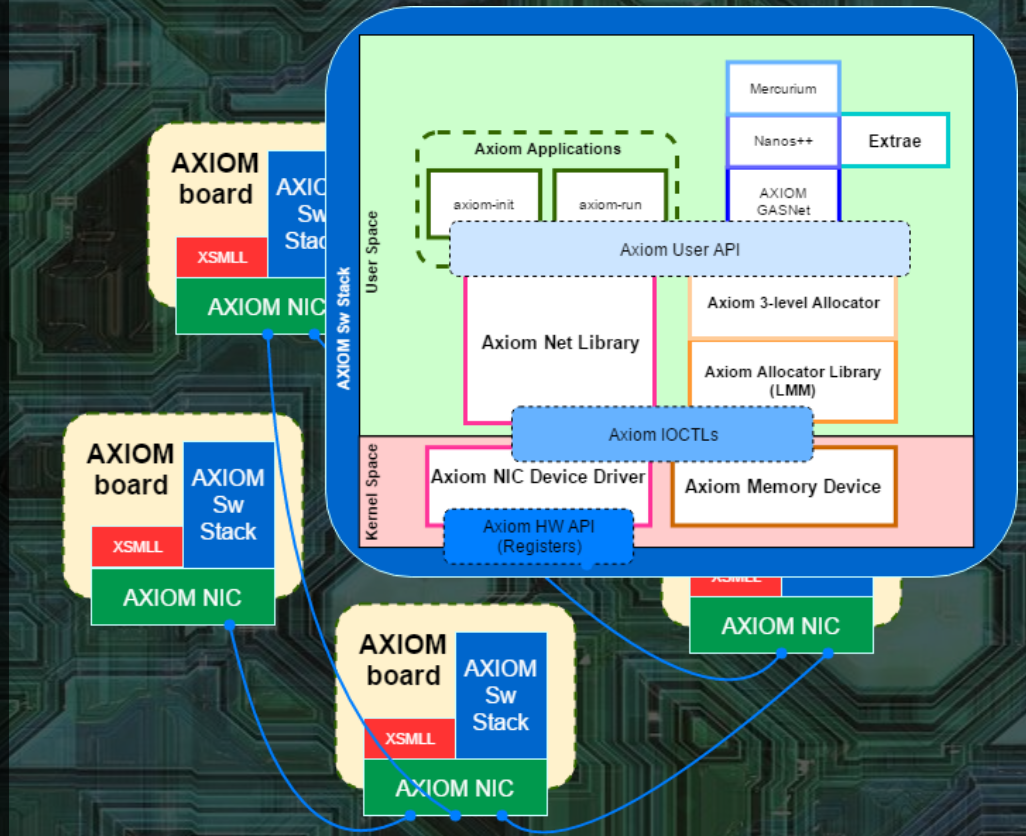
Cluster Software Architecture

- **Linux BSP** supporting on-board hardware
- **Libraries** to provide applications a convenient interface to hardware
- **User level applications** for system configuration
- **Remarkable examples**: AXIOM link, power monitors, memory allocation



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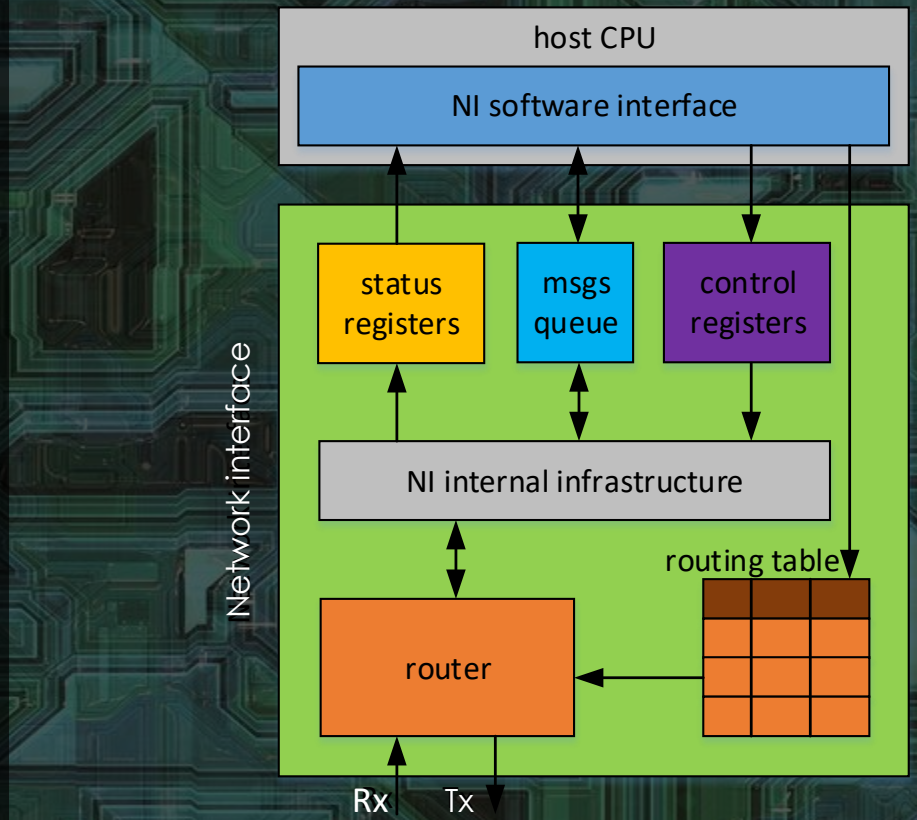
AXIOM LINK – NIC e SW I/F

- Support for **different topologies**: ring, 2D mesh, irregular
- Automatic link status monitoring and interconnect discovery
- Supports the transmission of 2 different message types
- **RDMA transfers**



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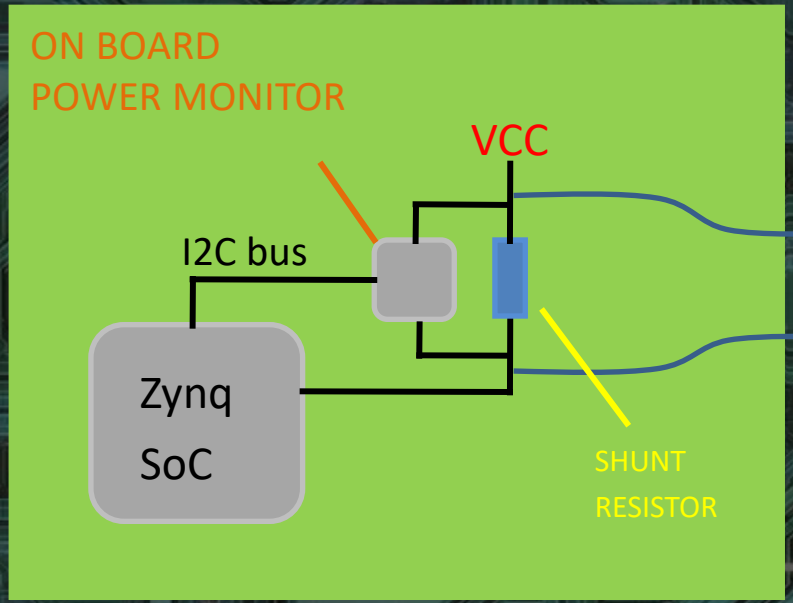
Power Monitoring and Profiling

Dedicated On-Board Hardware:

Power measurements on 8 supply rails
(70% of maximum total estimated power)

Specific Development Tools Cross Triggering Capabilities During Debug and Trace:

Dedicated test points for analog probe connections and ‘Breakpoint’ on given power consumption levels



- APPLICATIONS CAN TRACK POWER CONSUMTPION AGAINST RUNNING TASKS
- USERS MAY TEST CODING STYLES AGAINST POWER CONSUMPTION

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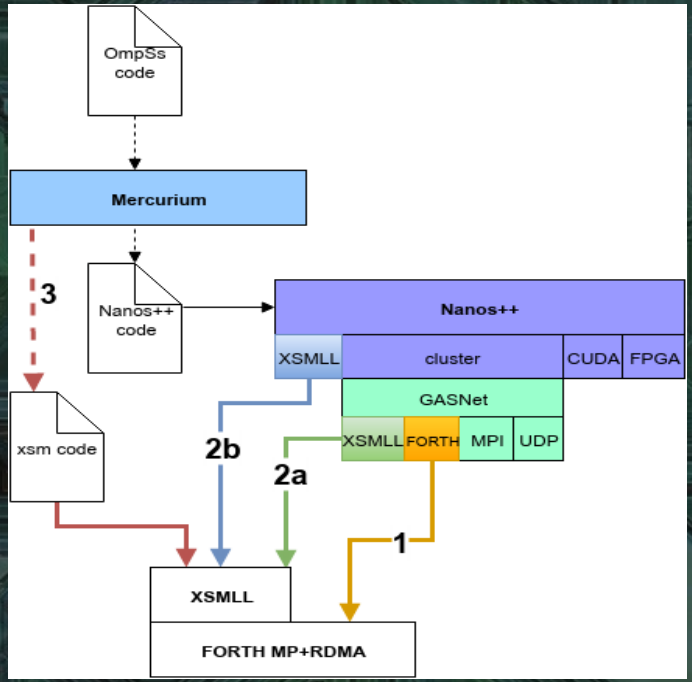
PROGRAMMING MODEL – OmpSs support

Exploit **parallel computation** of a sequentially written application over the AXIOM cluster.

- OmpSs@cluster
- OmpSs@FPGA

Specific extension of OmpSs components have been developed

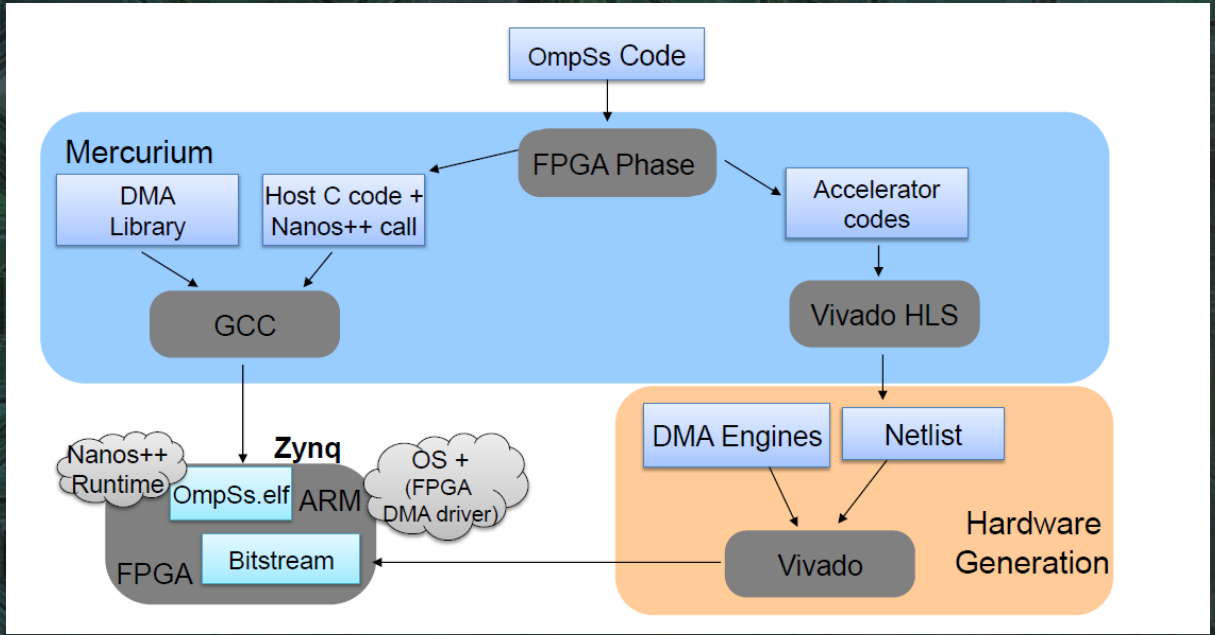


AXIOM Specific component was required at the networking layer (GASNet), a dedicated conduit has been developed

Programming Model – OmpSs support

OmpSs@FPGA

- New target in mercurium, in order to drive bitstream build with Vivado HLS compiler
- Runtime systems was adapted to spawn tasks to the FPGA and support data trasfers using a specifically developed DMA library



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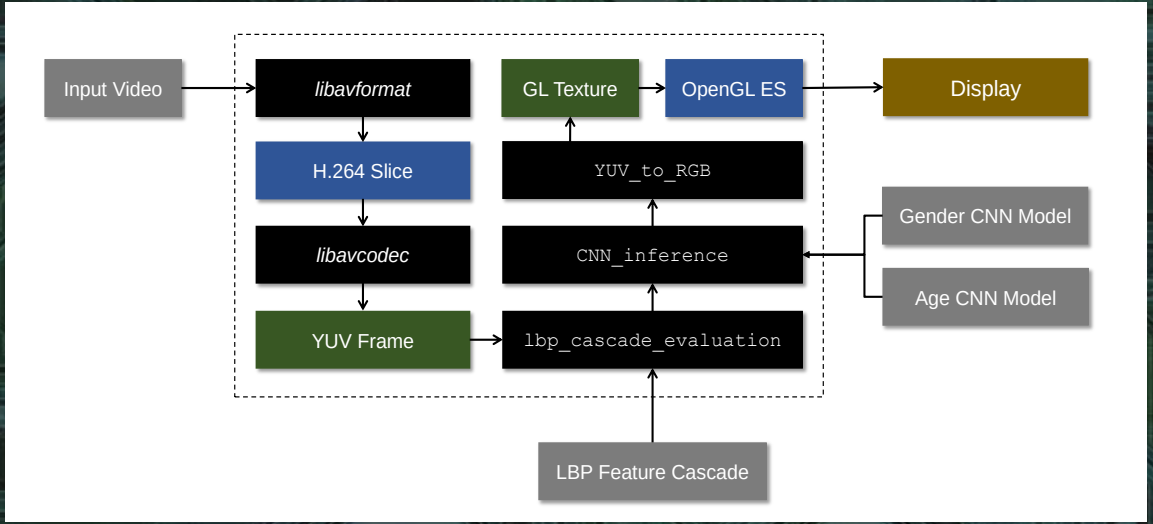
Proof of concept scenarios

SVS - face detection
for gender identification and age estimation

- **Security**
- **Customer profiling** for the retail sector



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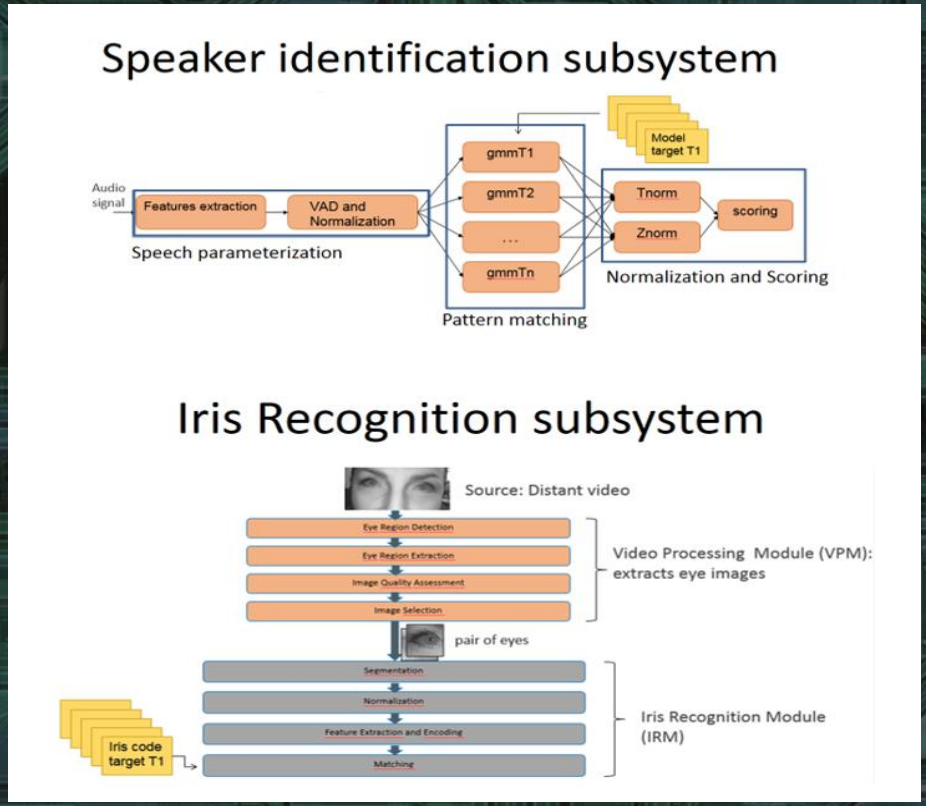
Proof of concept scenarios

Smart Home Living scenario - identification system which combines the analysis of two different biometrics:

- **Iris recognition**
- **Speaker identification**

The purpose of this scenario is to enforce the security of access while improving the interaction of the user with the smart home in a natural way.



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Intermediate results can be found @ http://www.axiom-project.eu/

Value proposition

- Minimal costs
- Hardware acceleration through **FPGA**
- Power efficient
- Reconfigurable

FLEXIBILITY

- Fast Interconnection
- Scalability
- Shrink HPC Clusters to the Embedded World
- Easy parallel programming

MODULARITY

Agile, e**X**tensible, fast **I/O** **M**odule for the cyber-physical era

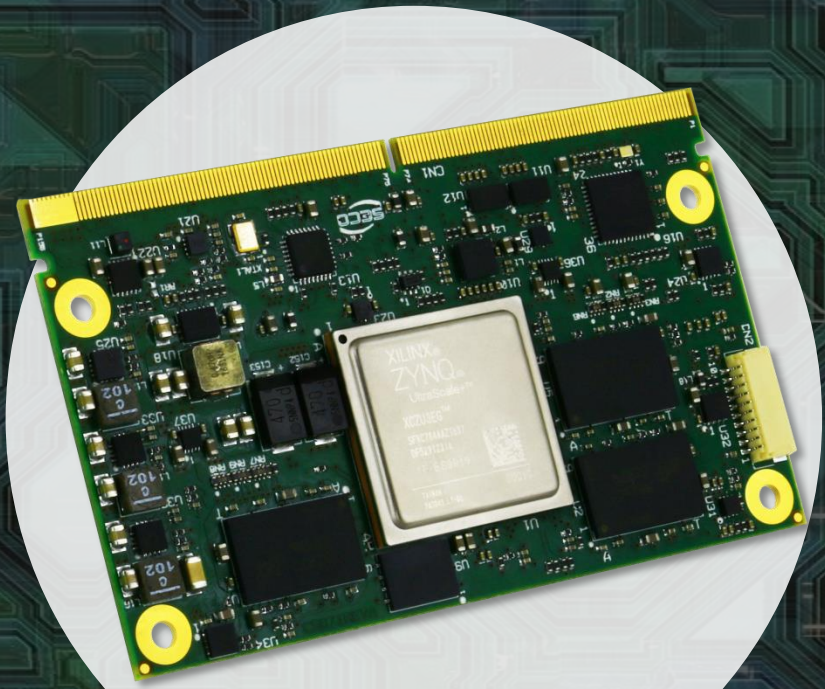
The first outcome for SECO

SM-B71: SECO industrial solution

SMARC compliant

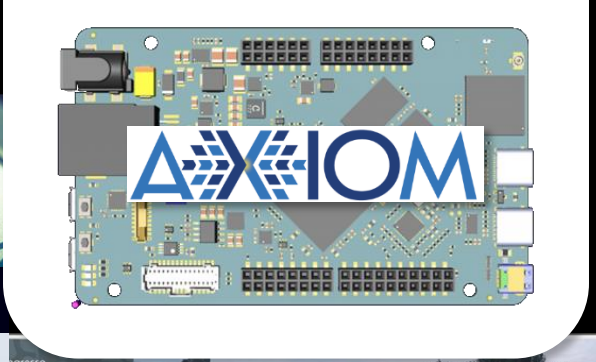
- Wide scalability from Dual-Core to Quad-Core ARM ® Cortex ®-A53 MPSoCs with GPU/VCU
- Dedicated Real-Time ARM® Cortex®-R5processors
- Extreme flexibility: up to 256k FPGA logic cells
- LVDS and DP video interfaces up to 4K resolution High-speed interfaces
- Dual memory interface (CPU/FPGA)
- MultiGb transceivers

modular solution

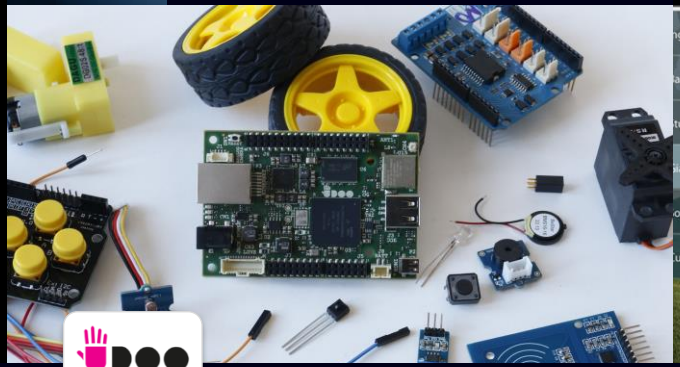


Out of the Lab

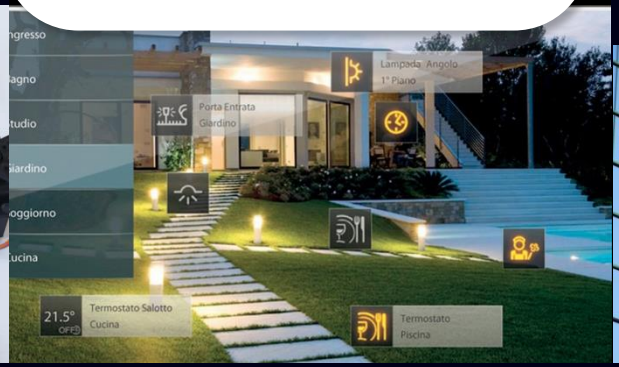
SMART HEALTH



SMART HOME



DO- IT-YOURSELF



SMART CAR

SMART ENERGY

SMART SURVEILLANCE

Thank you for your attention

www.seco.com