

http://www.axiom-project.eu

ICT-01-2014 GA 645496

Agile, eXtensible, fast I/O Module for the cyber-physical era



SMART CYBER-PHYSICAL SYSTEMS

START DATE: 01 Feb 2015

DURATION: 3 YEARS

EU FUNDING: 3'946 k €

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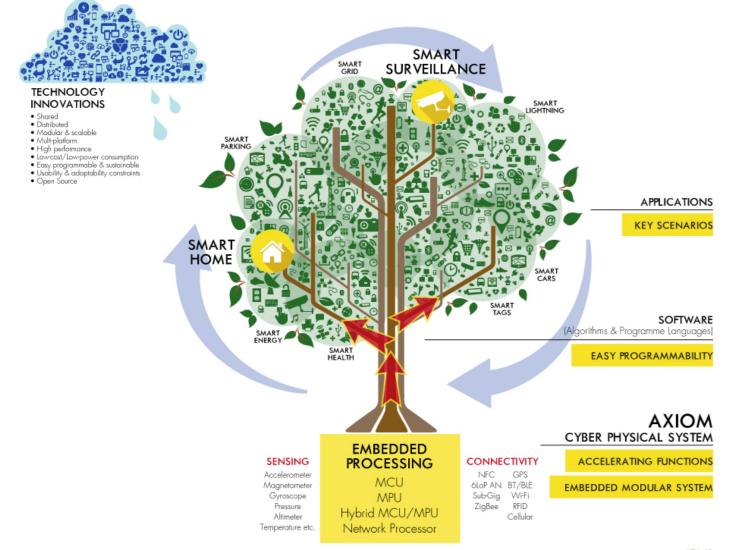


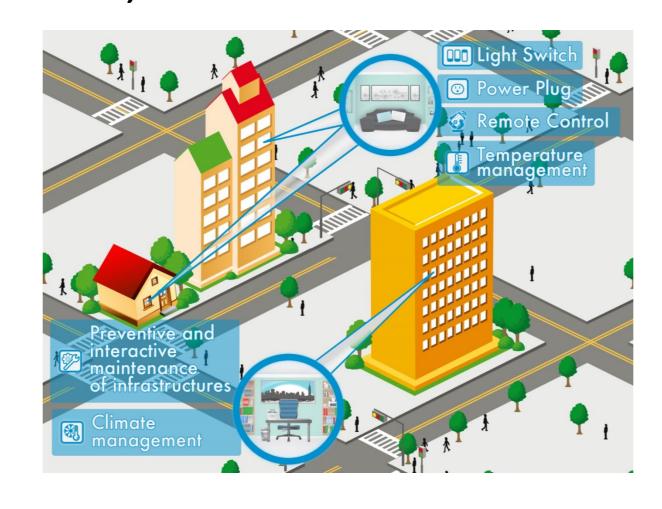




GOAL: EU HW/SW DESIGNED AND MANUFACTURED SINGLE-BOARD COMPUTER THAT CAN BECOME THE HEART OF FUTURE SMART APPLICATIONS

WP1: MANAGEMENT, WP2: DISSEMINATION, WP3: SCENARIO DEFINITION AND APPLICATION PORTING





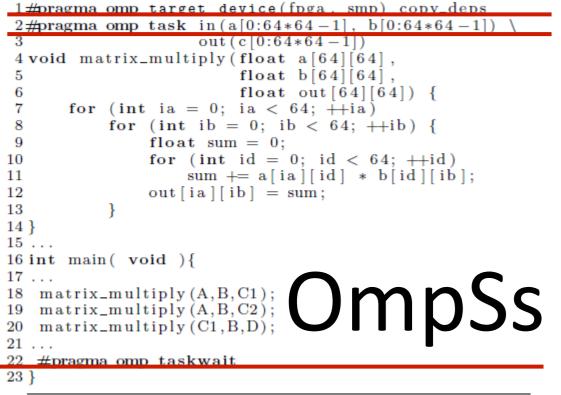


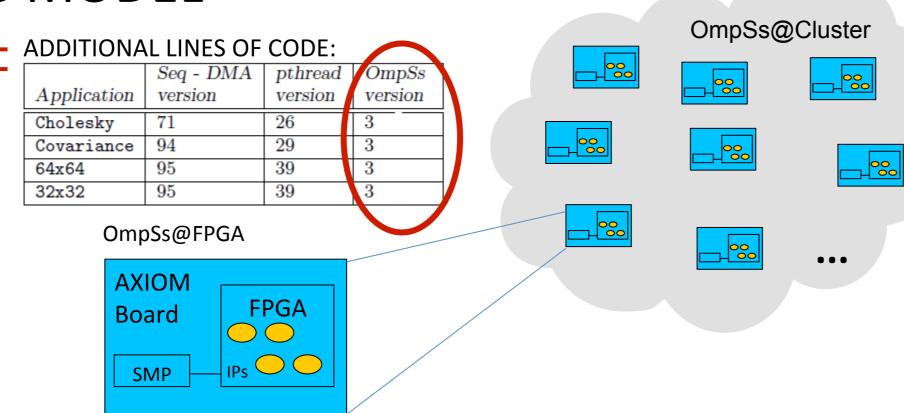
SMART HOME

AXIOM will enable companies, such as VIMAR, to improve real-time data analysis of its Energy Management catalogue and extend the network from the home to a large number of existing or near future services in collaboration with the municipality or even in a peer-to-peer scenario

SMART AXIOM will enable companies, such as HERTA, to deploy their multiple face recognition in real-time in crowded and changeable environments **VIDEOSURVEILLANCE**

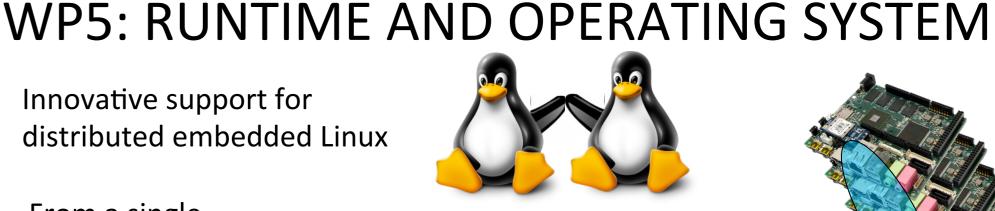
WP4: PROGRAMMING MODEL



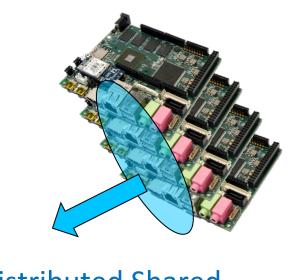


Innovative support for distributed embedded Linux From a single

embedded board...



...to a more powerful system made of small boards or modules



e.g., Distributed Shared Memory based concepts (to be explored further)

WP6: ARCHITECTURE IMPLEMENTATION, WP7: EVALUATION AND DESIGN SPACE EXPLORATION



THE AXIOM MODULE **KEY ELEMENTS:**

- K1: e.g., ZYNQ FPGA (INCLUDES DUAL ARM A9)
- K2: ARM GP CORE(S)
- K3: HIGH-SPEED & CHEAP INTERCONNECTS
- K4: SW STACK OMPSS+LINUX BASED
- K5: OTHER I/F (ARDUINO, USB, ETH, WIFI, ...)

INTEGRATING CONSORTIUM EXPERTISE

- VIMAR, HERTA 2 KILLER APPLICATIONS: SMART HOME AND SMART **VIDEOSURVELLANCE**
- SECO hardware module realization, architecture design
- FORTH high-speed interconnects, cost effective, ALL the way from IPC acceleration down to the customized data-link protocol and optimized packet formats
- EVI Runtime, OS (Linux 3.14 real time scheduler)
- BSC programming models
- UNISI simulation, evaluation, coordination, architecture

AXIOM OBJECTIVES

OBJ1) Realizing a small board that is flexible, energy-efficient and modularly scalable Flexibility: FPGA, fast-and-cheap interconnects based on existing connectors like SATA

- Energy efficiency: low-power ARM, FPGA
- Modularity: fast-interconnects, distributed shared memory across boards OBJ2) Easy programmability of multi-core, multi-board, FPGA
- Programming model: Improved OmpSs Runtime & OS: improved thread management

- **OBJ3) Leveraging Open-Source software to manage the board** • Compiler: BSC Mercurium, OS: Linux, Drivers: provided as open-source by partners
- **OBJ4) Easy Interfacing with the Cyber-Physical Worlds** Platform: integrating also Arduino support for a plenty of pluggable boards (so-called "shields")
- Platform: building on the UDOO experience of SECO

• Software: BSC is member of the OpenMP consortium

- **OBJ5) Enabling real time movement of threads** • Runtime: will leverage the EVIDENCE's SCHED DEADLINE scheduler (i.e. EDF)
- **OBJ6) Contribution to Standards** · Hardware: SECO is founding member of the Standardization Group for Embedded Systems (SGET)

included Linux 3.14, UNISI low-level thread management techniques

TOWARDS HPC+EMBEDDED CONVERGENCE

