

http://www.axiom-project.eu ICT-01-2014 GA 645496

Agile, eXtensible, fast I/O Module for the cyber-physical era



START DATE: 01 Feb 2015 **DURATION: 3 YEARS** EU FUNDING: 3'946 k €

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(Coordinator Partner)









VIMAR-ELVOX

Video Door

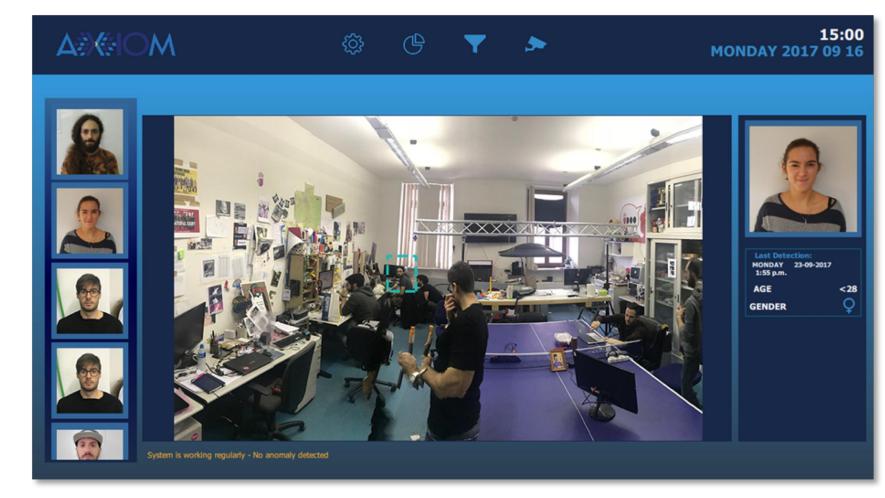


GOAL: EU HW/SW DESIGNED AND MANUFACTURED SINGLE BOARD COMPUTER THAT CAN BECOME THE HEART OF FUTURE SMART APPLICATIONS

WP1: MANAGEMENT, WP2: DISSEMINATION, WP3: SCENARIO DEFINITION AND APPLICATION PORTING



Entry System VIMAR User Interface **AXIOM** Board



PRESENTED AT



THE EUROPEAN EDITION

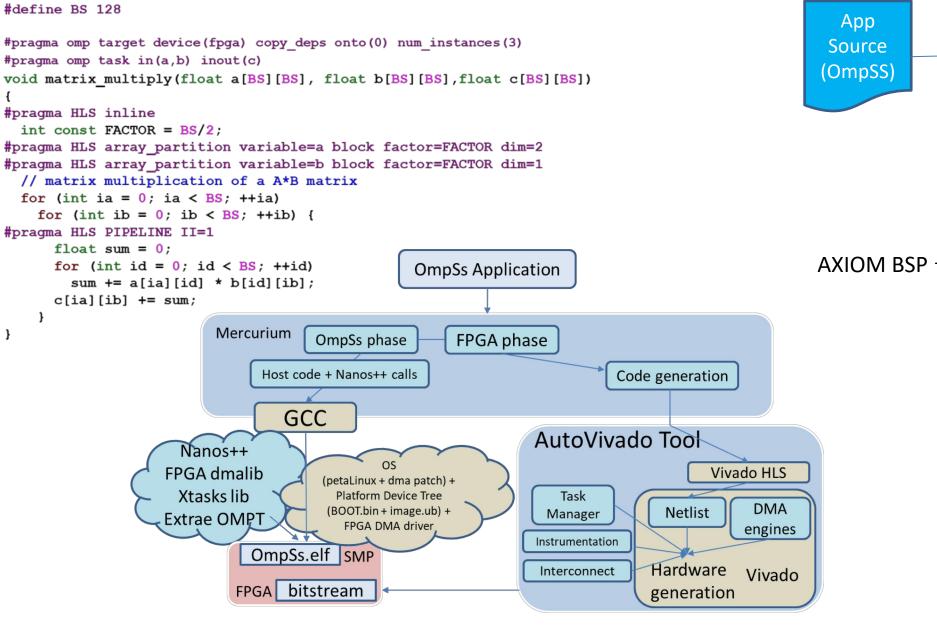


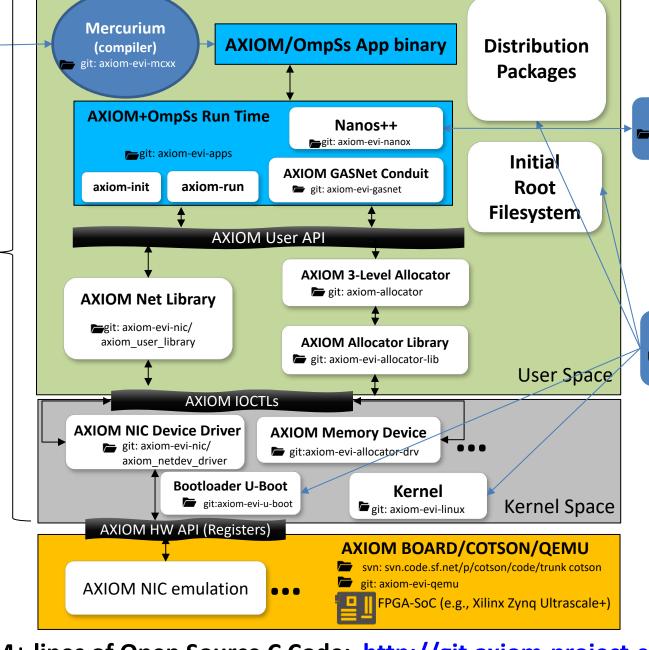


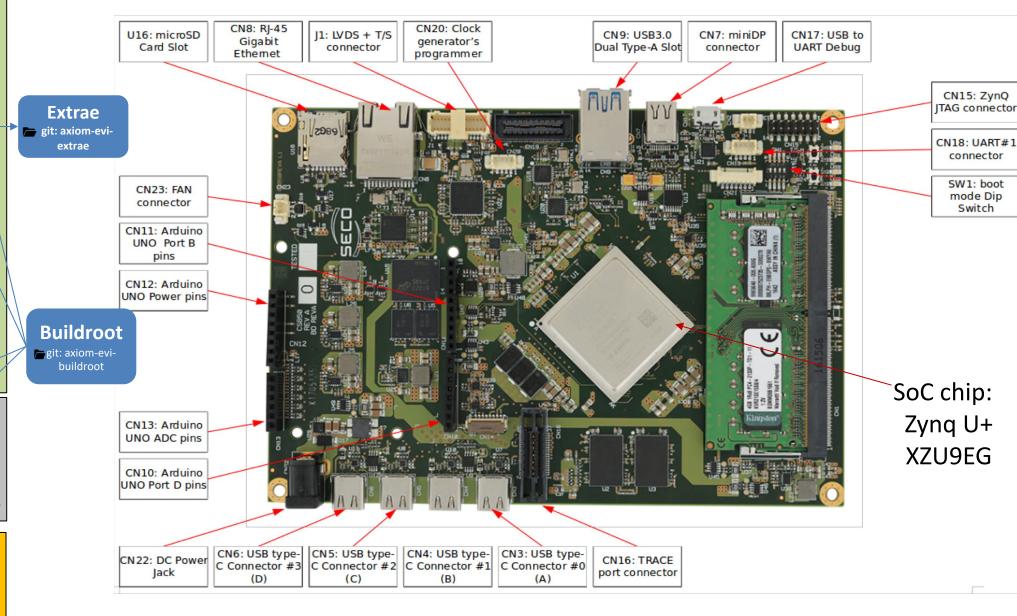
SMART AXIOM enables companies, such as VIMAR, to improve real time data analysis of its Energy Management catalogue and to extend the network from the home to a large number HOME of existing or near future services.

SMART AXIOM enables companies, such as HERTA, to deploy their multiple face recognition in real-time in crowded and changeable environments VIDEOSURVEILLANCE

WP4: Programming Model, WP5: RUNTIME AND OPERATING SYSTEM, WP6: ARCHITECTURE IMPLEMENTATION





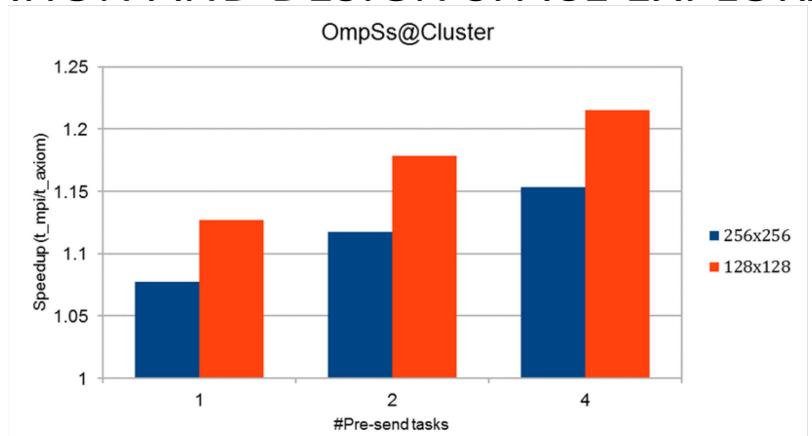


AUTOVIVADO tool: see https://pm.bsc.es/ompss-at-fpga for more info

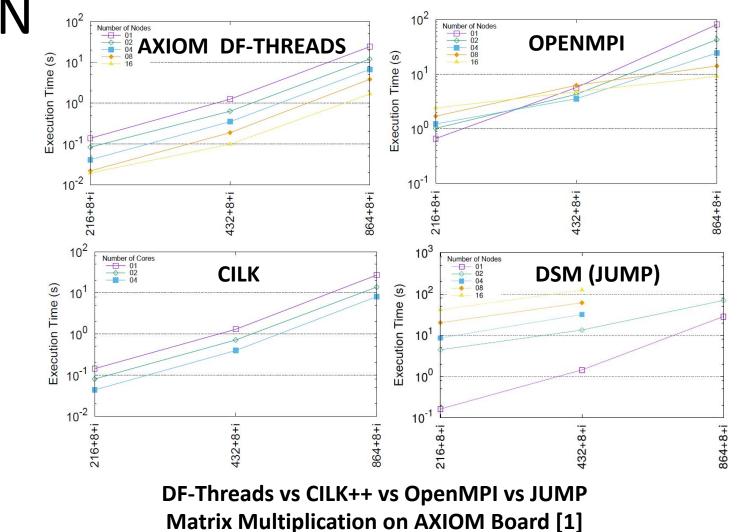
1M+ lines of Open Source C Code: http://git.axiom-project.eu

WP7: EVALUATION AND DESIGN SPACE EXPLORATION →Single transfer →32 Async transfers 20 20 18 10 = 250 25000 250000 PAYLOAD SIZE (BYTES)

RDMA write / read throughput between two nodes: 18 Gbps!



OmpSs@Cluster Matrix Multiplication AXIOM NIC vs MPI Ethernet



AXIOM OBJECTIVES

Runtime & OS: improved thread management

OBJ1) Realizing a small board that is flexible, energy efficient and modularly scalable • Flexibility: FPGA, fast-and-cheap interconnects based on existing connectors like SATA

- · Energy efficiency: low-power ARM, FPGA · Modularity: fast-interconnects, distributed shared memory across boards
- OBJ2) Easy programmability of multi-core, multi-board, FPGA • Programming model: Improved OmpSs

• Compiler: BSC Mercurium, OS: Linux, Drivers: provided as open-source by partners **OBJ4) Easy Interfacing with the Cyber-Physical Worlds**

OBJ3) Leveraging Open-Source software to manage the board

- Platform: integrating also Arduino support for a plenty of pluggable board (so-called "shields") Platform: building on the UDOO experience from SECO
- **OBJ5) Enabling real time movement of threads** • Runtime: will leverage the EVIDENCE's SCHED DEADLINE scheduler (i.e. EDF) included Linux 3.14, UNISI low-level thread management techniques

• Software: BSC is member of the OpenMP consortium

OBJ6) Contribution to Standards • Hardware: SECO is founding member of the Standardization Group for Embedded Systems (SGET)

TOWARDS HPC+EMBEDDED CONVERGENCE

