AXIOM: Enabling Parallel-Processing in Cyber-Physical Systems

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What is AXIOM?

Agile, e**X**tensible, fast **I**/**O M**odule
 started in Feb. 2015

Aim: develop a new HW/SW CPS architecture for that support heavy interaction w/ humans

- Real-time system reaction
- Ample computational power
- Energy efficiency
- Modularity & scalability
- Easy programmability

Project Consortium

Academic: U. Siena, BSC, FORTH

Industrial: Evidence, Herta Security, SECO, VIMAR

Outline

- Motivation/Objectives

- The AXIOM Platform

- Programming Model

- Network Interconnect

- Application Domains

- Conclusions

Motivation

- UDOO development board
  - Funded by two partners
  - ARM quad-core, Arduino 2 I/F
  - Kickstarter project

- Push this idea further

- *Goal: A European -designed and manufactured- single board computer: The heart of future smart applications*
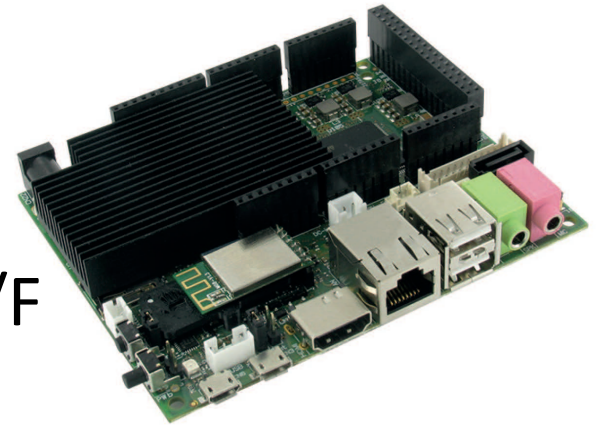
Project Objectives

Design and build an affordable ARM + FPGA board (now based on the latest Ultrascale+) :

- Flexible, energy efficient, scalable, modular
- Multi-core + ***Acceleration*** + Multi-board programmability with OmpSs
- Arduino shields for interfacing with CPS world
- Efficient & High-speed networking
- Distributed Shared Memory support
- Contribution to standards? OpenMP, SGET,…

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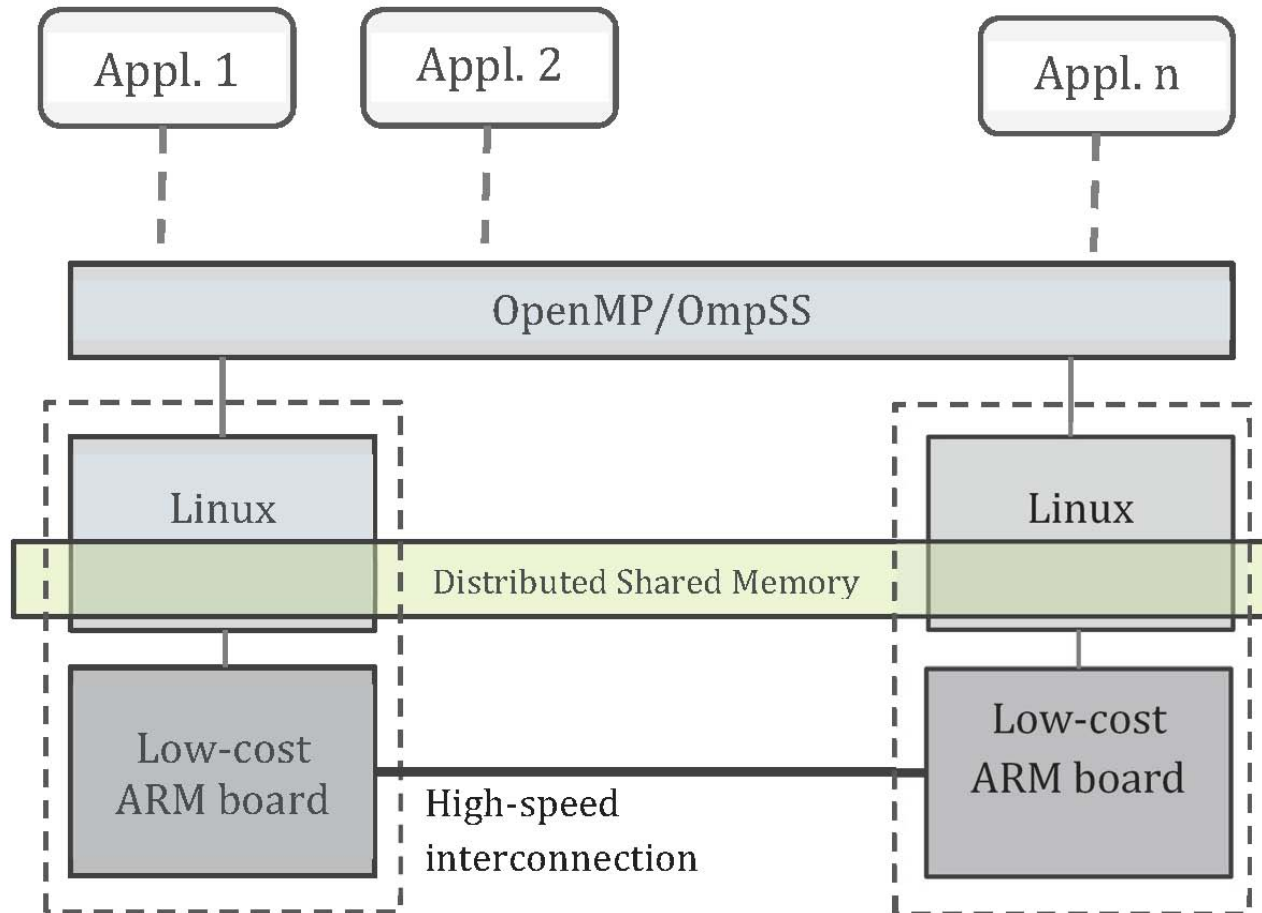
The AXIOM Platform

The AXIOM Platform (cntd)

Current *prototyping* board (ZC706):

Zynq 7045 SoC (2-core ARM+Kintex7 fabric), 16 high-speed transceivers
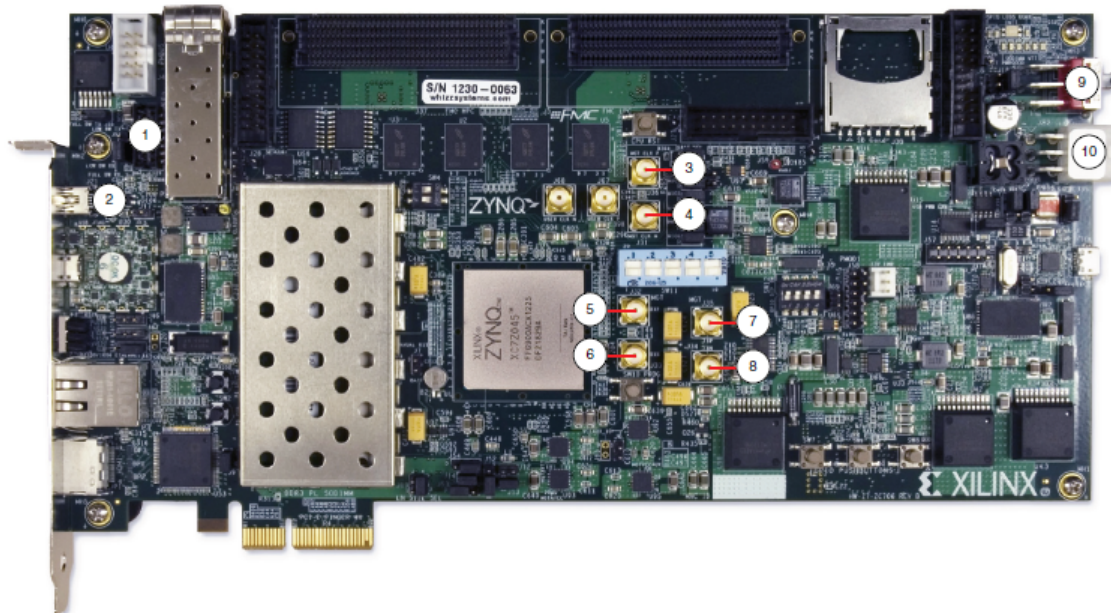
The AXIOM Platform (cntd)

Next *prototyping* board

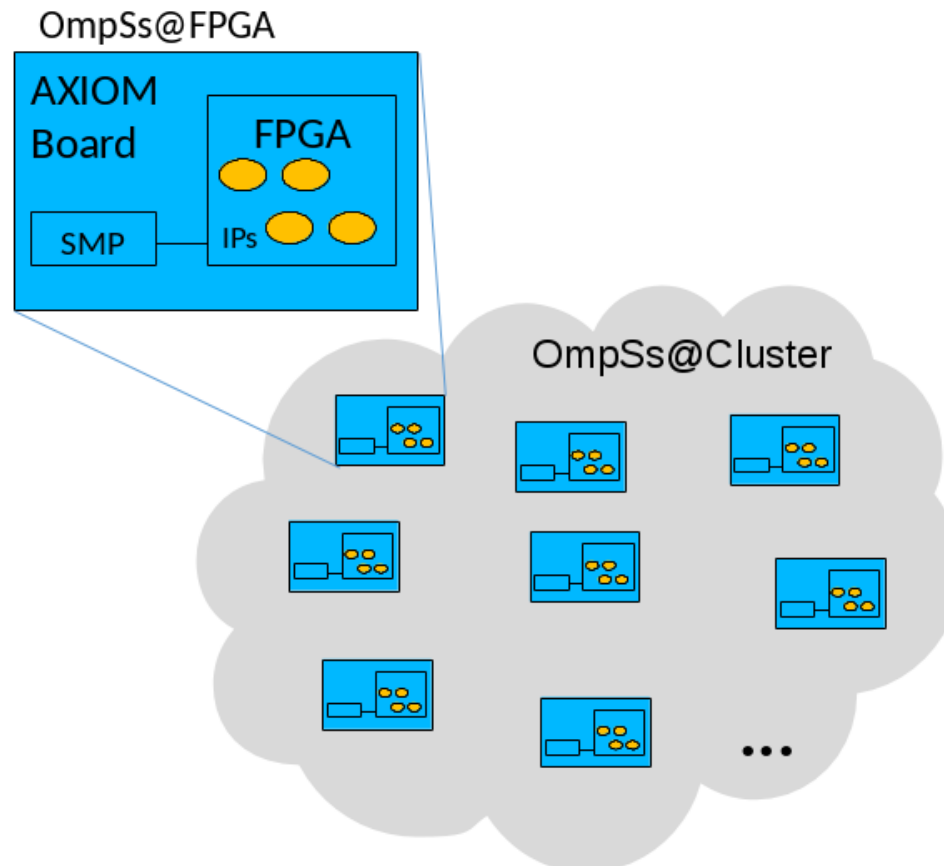○ UltraScale+ Trenz Electronic TE0808

Programming Model

- Leverage on OmpSs framework
  - Mercurium compiler (C/C++, Fortran)
  - Nanos++ runtime system
  - Task-based programming model
- <u>Programming</u>
  - **<u>Intra</u>-<u>node:</u>** OmpSs@FPGA
  - **<u>Inter</u>-<u>node:</u>** Explore OmpSs@Cluster and DSM-like solutions

Programming Model (cntd)

○ OmpSs@FPGA + OmpSs@Cluster

Programming Model (cntd)

- OmpSs on DSM-like systems
  - Reliable and efficient DSM mechanism
  - OmpSs@FPGA: intra-node programming
  - OmpSs@Cluster: single OmpSs intra-node running over a transparent DSM system
  - Integrated to Linux, Open-Source

Network Interconnect

Challenge: low cost but high-performance!
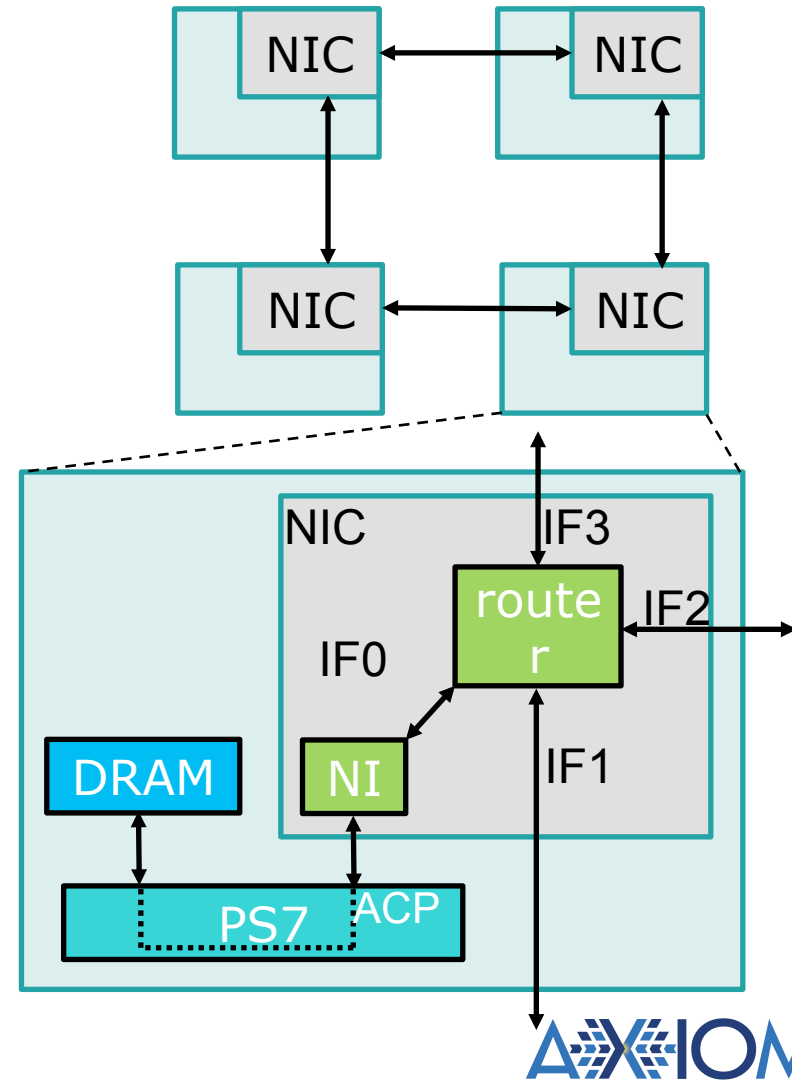
Board-2-board interconnections:

- Use cheap SATA connectors(?)
- High-speed links: 6+ Gbit/sec
- rDMA support
- Low-level communication interface to support OmpSs@cluster and DSM-like programming approaches

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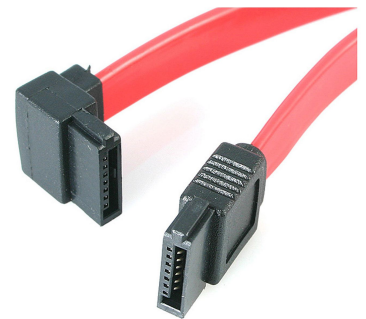
Network Interconnect (cntd)
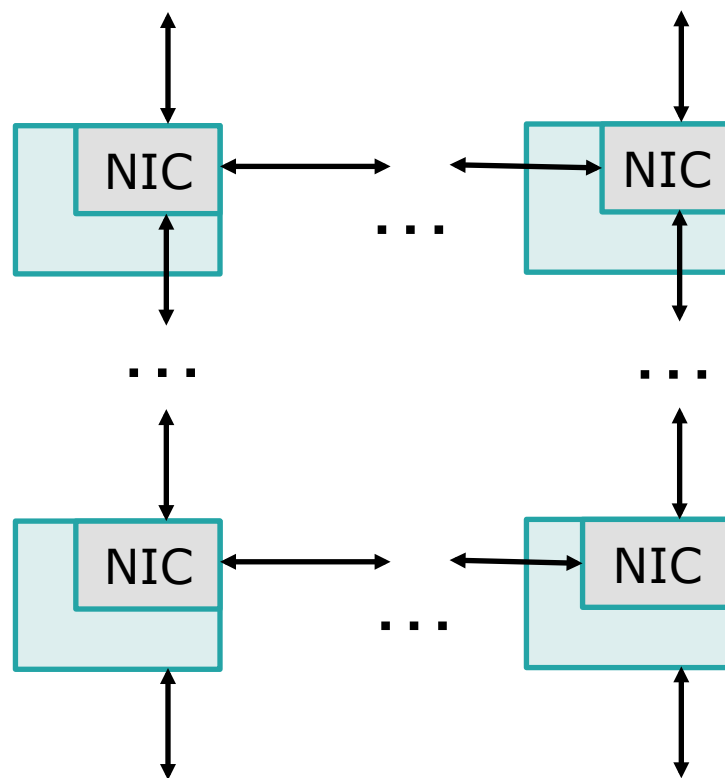
Ring topology

- 1 input/1 output per AXIOM board

- Simple on-board routing, suitable for small networks

- Simple interconnection wiring!

Network Interconnect (cntd)
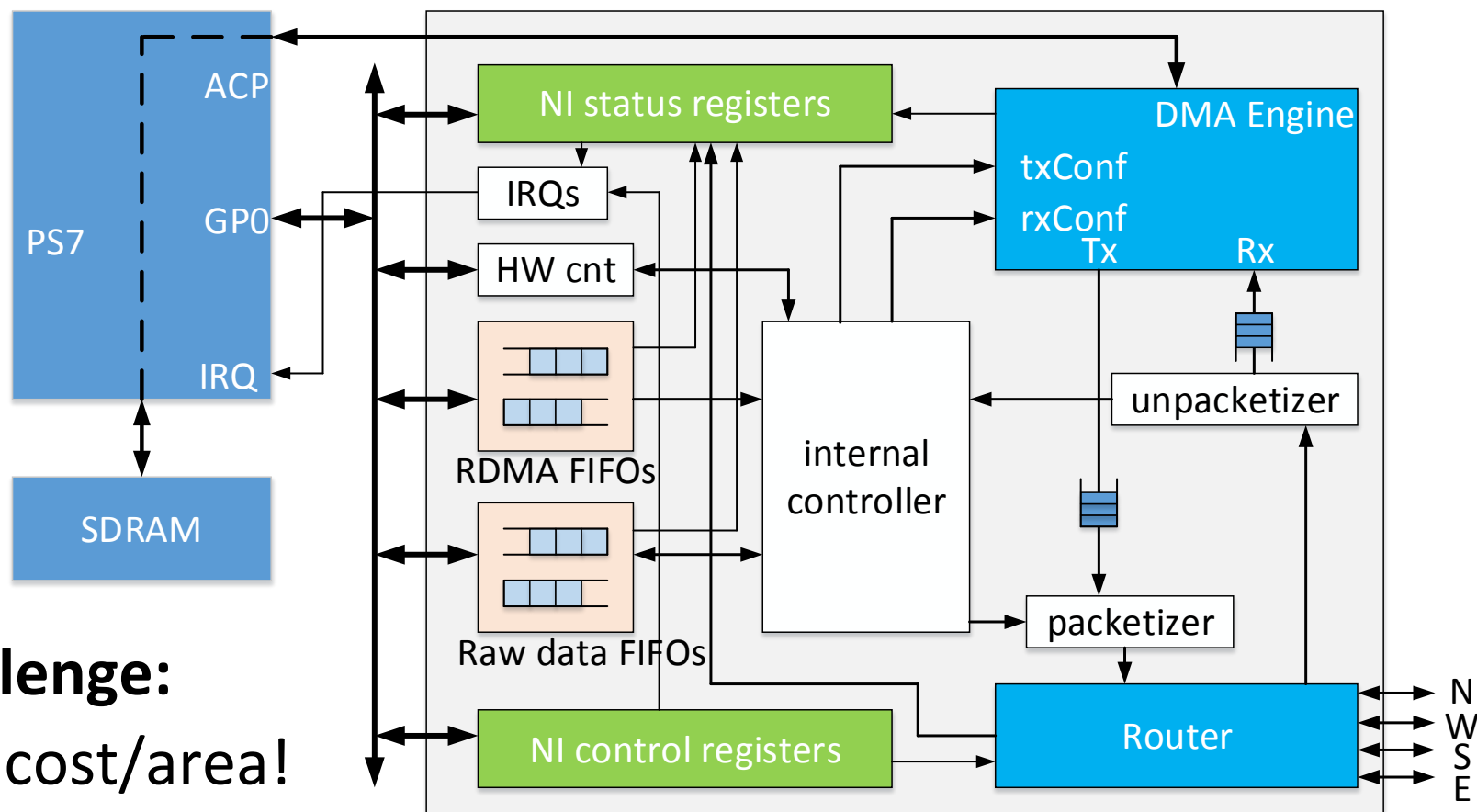
2D mesh/torus topology

- 2 inputs/2 outputs per AXIOM board
- X-Y routing
- Suitable for larger networks
- More complex wiring…

Ad-hoc topology support?

Network Interconnect (cntd)

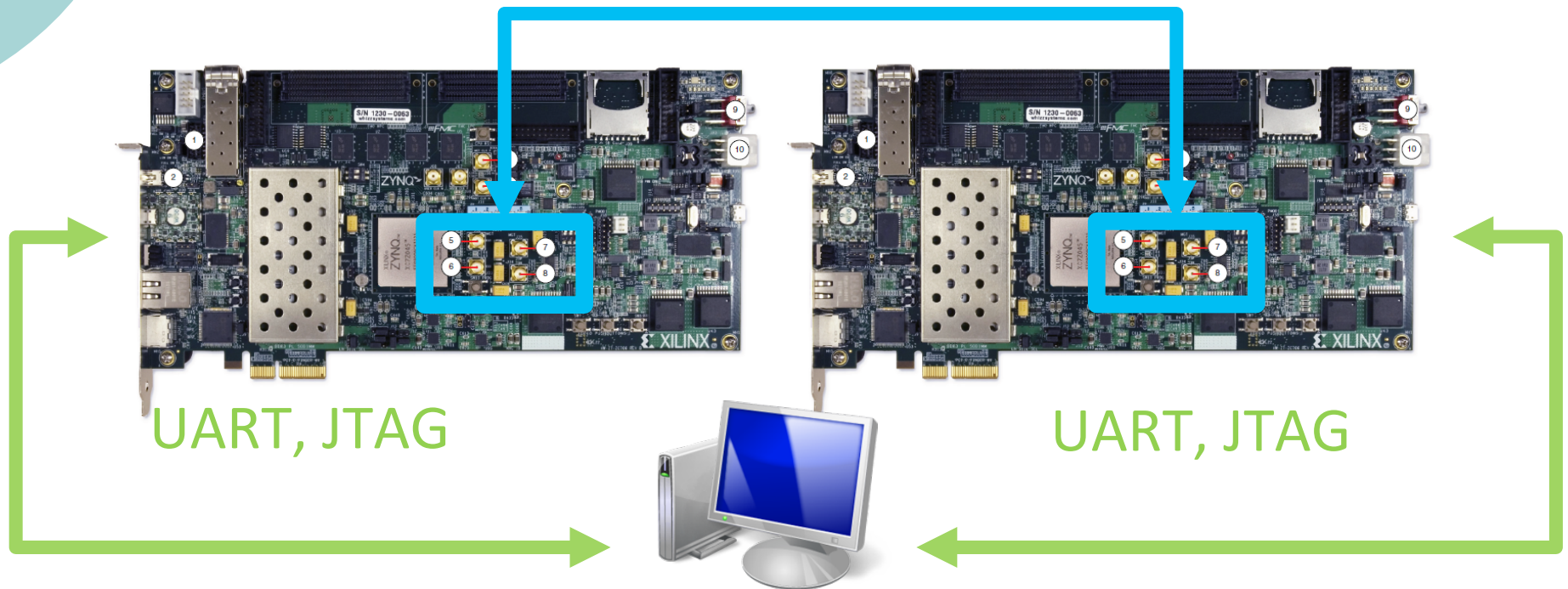## Network Interface Block Diagram

Challenge:

Low cost/area!

Network Interconnect (cntd)
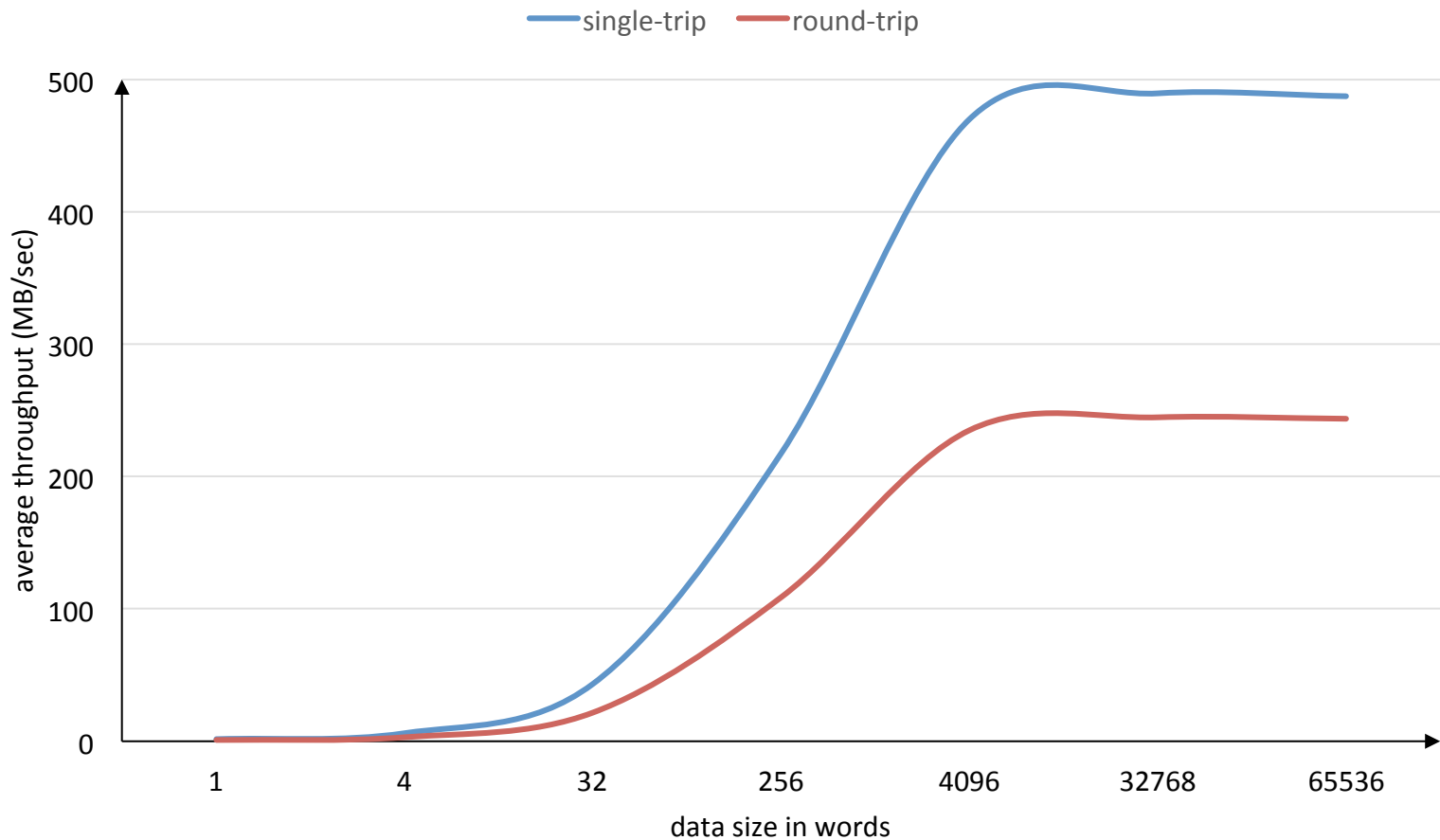
Connectivity evaluation setup (on Zynq)

○ Bare metal, run SW kernel

SMA cables

UART, JTAG

UART, JTAG

Network Interconnect (cntd)

Initial results

Application Domain: Video Surveillance

Intelligent, multi-camera, computer vision & pattern recognition

Challenge: *huge* amounts of video

Applications: Homeland security, traffic control, accident prediction and detection, targeted advertisement, etc.

Application Domain: Smart Home

Ambient intelligence and automatic control for property/residence management

- ○ Different type of data are gathered by sensors

- ○ Data analysed to control certain built-in mechanisms (e.g. room lighting)

Conclusions

- AXIOM targets a *European-designed and -manufactured single board computer*

- Scalable platform with high-speed interconnect & sophisticated NI functionality

- Intra- and inter-node programmability with the OmpSs framework

- Acceleration infrastructure

- Board development on-going

- (AXIOM) CPSs will be the heart of future smart applications

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Thank you!

Questions?