AXIOM

Agile, eXtensible, fast I/O Module for the cyber-physical era

Advanced Computing and Cyber-Physical SystemCollaboration Workshop

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Brief introduction to the AXIOM project

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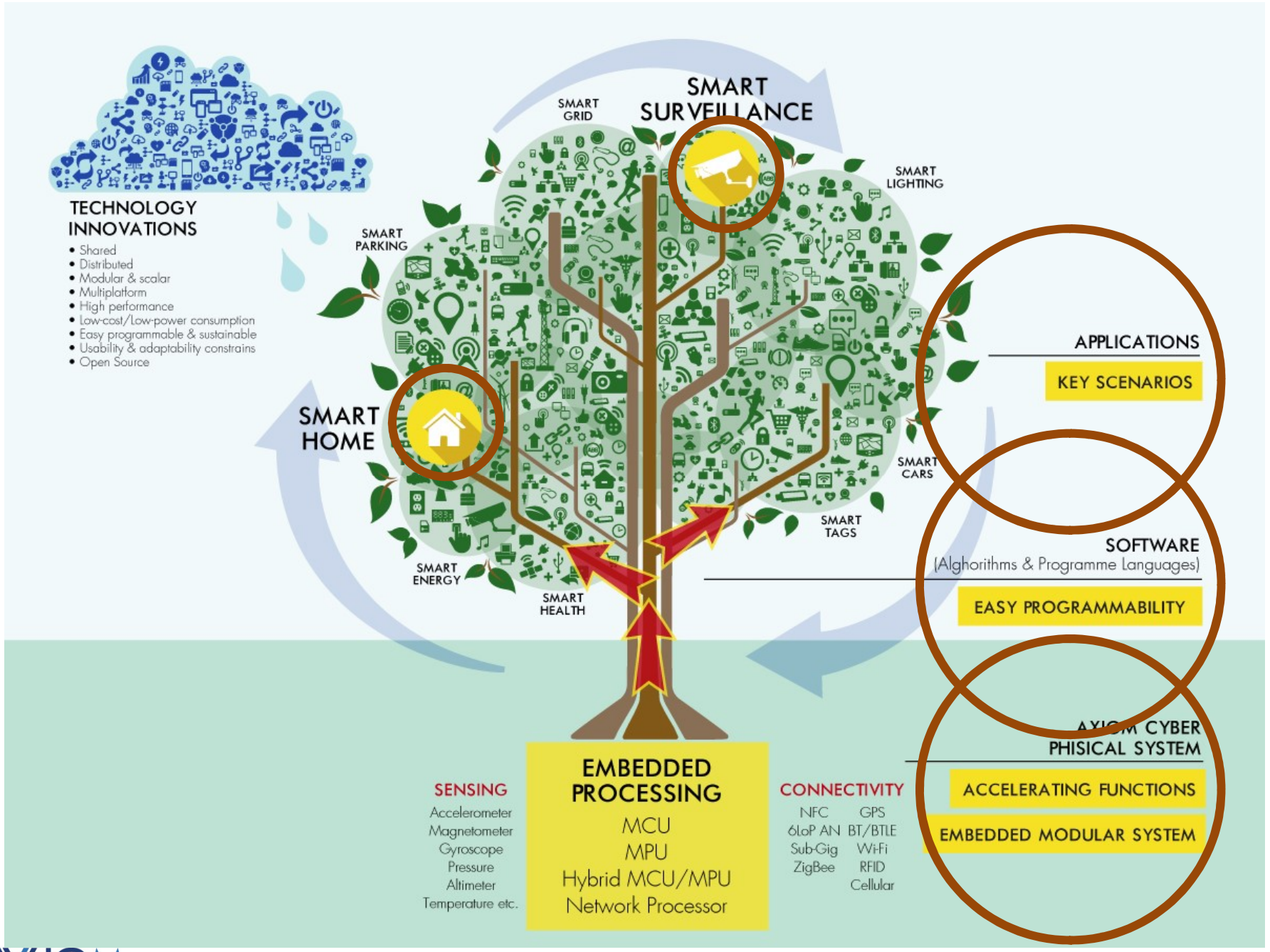

TECHNOLOGY INNOVATIONS
• Shared
• Distributed
• Modular & scalar
• Multiplatform
• High performance
• Low-cost/Low-power consumption
• Easy programmable & sustainable
• Usability & adaptability constrains
• Open Source
SMART GRID
SMART SURVEILLANCE
SMART LIGHTING
SMART PARKING
SMART HOME
SMART CARS
SMART TAGS
SMART ENERGY
SMART HEALTH
APPLICATIONS
KEY SCENARIOS
SOFTWARE
(Alghorithms & Programme Languages)
EASY PROGRAMMABILITY
AXIOM CYBER PHISICAL SYSTEM
ACCELERATING FUNCTIONS
EMBEDDED MODULAR SYSTEM
SENSING
Accelerometer
Magnetometer
Gyroscope
Pressure
Altimeter
Temperature etc.
EMBEDDED PROCESSING
MCU
MPU
Hybrid MCU/MPU
Network Processor
CONNECTIVITY
NFC
6LoP AN
Sub-Gig
ZigBee
GPS
BT/BTLE
Wi-Fi
RFID
Cellular

AXIOM OBJECTIVES

- **OBJ1) Realizing a small board that is flexible, energy efficient and modularly scalable**
  - Flexibility: FPGA provides acceleration, custom interconnects, ability to distribute threads across boards
  - Energy efficiency: low-power ARM, FPGA
  - Modularly scalable: fast+inexpensive interconnects based on SATA/USB-C, distributed shared memory across boards
- **OBJ2) Easy programmability of multi-core, multi-board, FPGA**
  - Programming model: Improved OmpSs
  - Runtime & OS: improved thread management
- **OBJ3) Leveraging Open-Source software to manage the board**
  - Compiler: BSC Mercurium
  - OS: Linux
  - Drivers: provided as open-source by partners
- **OBJ4) Easy Interfacing with the Cyber-Physical World**
  - Cyber-Physical World: integrating Arduino support for a plenty of pluggable board (so-called “shields”)
  - Platform: building on the UDOO experience from SECO
- **OBJ5) Enabling real time movement of threads**
  - Runtime: will leverage the EVIDENCE’s SCHED_DEADLINE scheduler (i.e. EDF) included Linux 3.14, UNISI’s low-level dataflow-based thread management techniques
- **OBJ6) Contribution to Standards**
  - Hardware: SECO is founding member of the Standardization Group for Embedded Systems (SGET)
  - Software: BSC is member of the OpenMP consortium

EASY PROGRAMMABILITY VIA OPENMP-SS (OMPSS)

```
1 #pragma omp target device(fpga, smp) copy_deps
2 #pragma omp task in(a[0:64*64-1], b[0:64*64-1]) \
3                  out(c[0:64*64-1])
4 void matrix_multiply(float a[64][64],
5                       float b[64][64],
6                       float out[64][64]) {
7     for (int ia = 0; ia < 64; ++ia)
8         for (int ib = 0; ib < 64; ++ib) {
9             float sum = 0;
10            for (int id = 0; id < 64; ++id)
11                sum += a[ia][id] * b[id][ib];
12            out[ia][ib] = sum;
13        }
14 }
15 ...
16 int main( void ){
17 ...
18  matrix_multiply(A,B,C1);
19  matrix_multiply(A,B,C2);
20  matrix_multiply(C1,B,D);
21 ...
22  #pragma omp taskwait
23 }
```

Only 3 lines of code to
- accelerate code on FPGAs
- distributed code across several AXIOM boards

Application	*Seq - DMA version*	*pthread version*	*OmpSs version*
Cholesky	71	26	3
Covariance	94	29	3
64x64	95	39	3
32x32	95	39	3

CAN WE DO THAT ?

- SECO/UNISI achievements:
  - 2014: UDOO-ARM (99 $ PC+Arduino) → 600k$ on Kickstarter
  - 13th April 2016: UDOO-x86 (PC+Arduino, 10x faster than Raspberry-3) → 100k$ in 7 hours (!) on Kickstarter

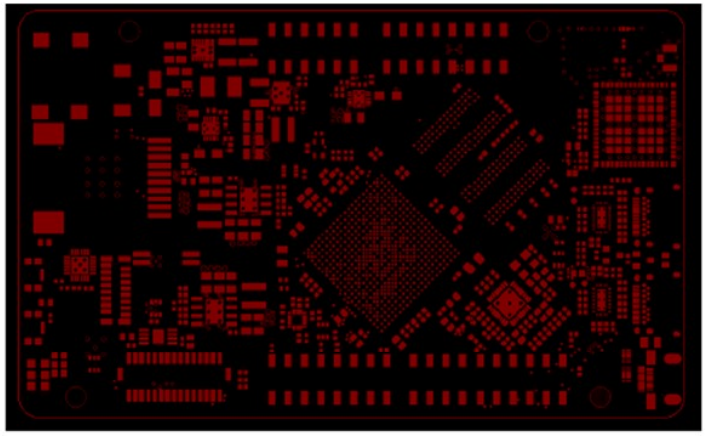
UDOO X86 FOR CLUSTER

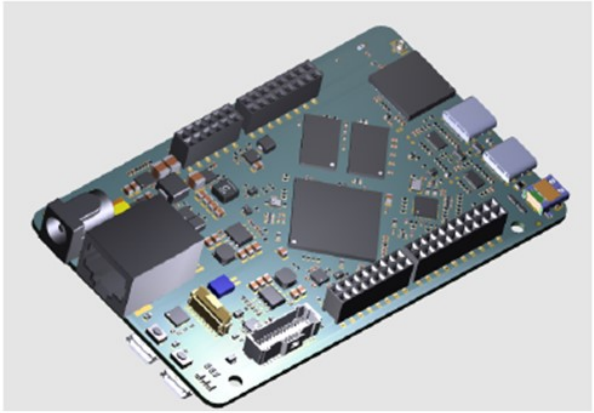
POWERED BY OmpSs
THANKS TO AXIOM

AXIOM

FIRST PROTOTYPE UNDER REVIEW

- Stackup definition
  - 10 layers PCB
  - HS/LS/power planes arrangement
- Placement
  - Achieve mechanical and electrical constraints
- Routing (WIP)
  - Design for power/signal integrity
- 3D model available





AXIOM – THE MODULE-v2

- KEY ELEMENTS
  - K1: ZYNQ FPGA (INCLUDES 6 ARM CORES)
  - K2: ARM GP CORE(S)
  - K3: HIGH-SPEED & INEXPENSIVE INTERCONNECTS
  - K4: SW STACK – OMPSS+LINUX BASED
  - K5: OTHER I/F (ARDUINO, USB, ETH, WIFI, …)

CONSORTIUM EXPERTISE

- VIMAR, HERTA – 2 KILLER APPLICATIONS
- SECO – hardware module realization
- FORTH – high-speed interconnects
- EVI – Runtime, OS (Linux 3.14 real time scheduler)
- BSC – programming models
- UNISI – simulation, evaluation, coordination, architecture

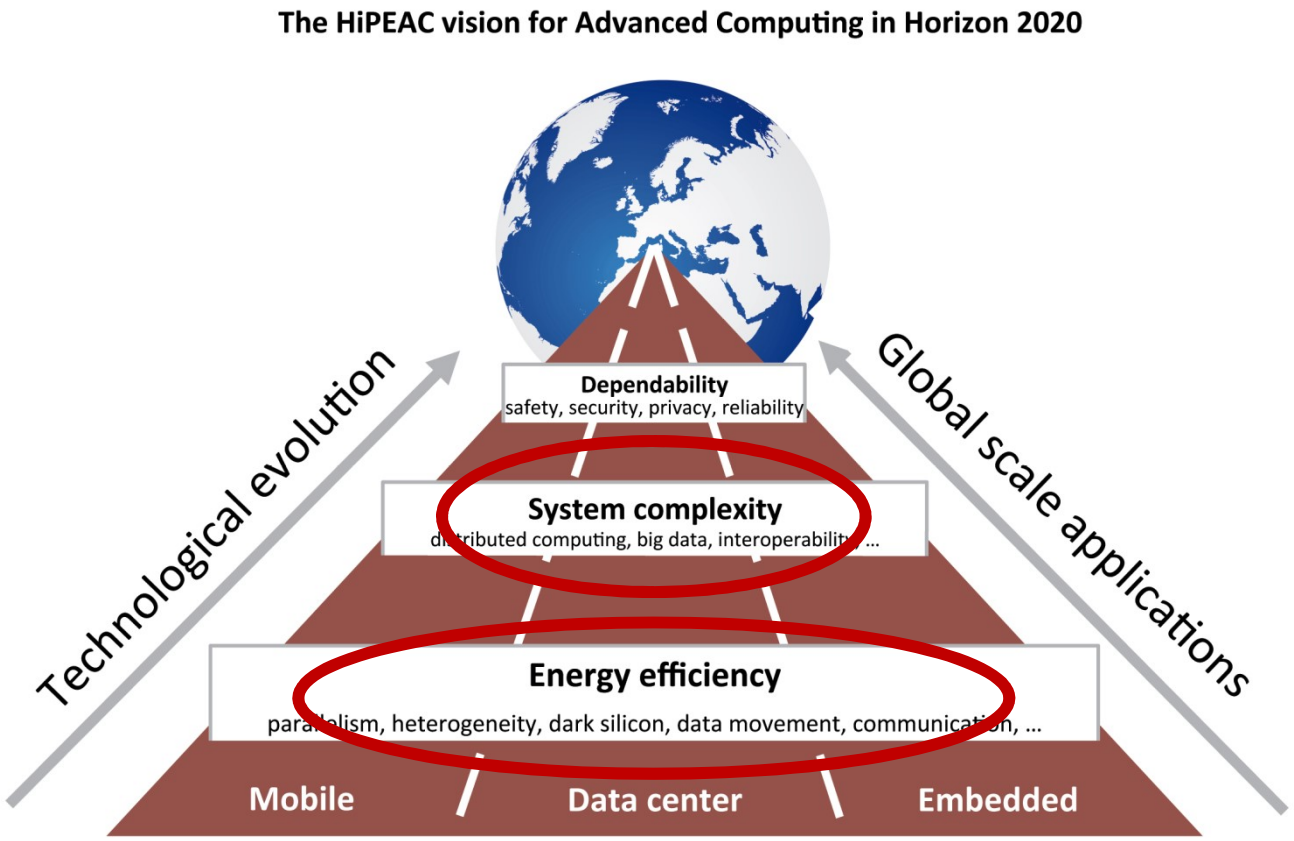
WORKPACKAGES

- WP1: **Management** – UNISI (leader-Macy-project manager),
  ALL partners (mandatory)
- WP2: **Dissemination and Exploitation** – UNISI (leader-Caporali),
  ALL partners
- WP3: **Scenario Definition and App. Porting** – UNISI (leader-Rizzo),
  VIMAR, HERTA
- WP4: **Programming Model** – BSC (leader-Martorell),
  EVI, FORTH, SECO, HERTA
- WP5: **Runtime and OS** – EVI (leader-Gai),
  BSC, FORTH, SECO, UNISI
- WP6: **Platform** – SECO (leader-Catani),
  BSC, EVI, FORTH, UNISI, VIMAR
- WP7: **Simulation and Evaluation** – UNISI (leader-Giorgi),
  ALL partners

CONCLUSION - AXIOM IMPACT

- Realize a prototype module “ready-for-market”
  - VIMAR, HERTA first customers
    - for the public afterwards
- Strengthen European industry and research
  - in the supply, operate and use of Embedded Systems, achieving world-leadership
  - development of autonomous technology
- Development of extreme-performance system software and tools
  - European research at the forefront

TOWARDS
HPC + EMBEDDED CONVERGENCE



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PROJECT ID: 645496

University of Siena
(Coordinator Partner)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EVIDENCE
EMBEDDING TECHNOLOGY

herta security

FORTH
Institute of Computer Science

SECO

VIMAR
energia positiva