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Agile, eXtensible, fast I/O Module for the cyber-physical era

D1.1 – Technical specification of AXIOM boards

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GLOSSARY

eMMC – Embedded Multi Media Card

FPGA – Field Programmable Gate Array

MGT – Multi-Gigabit Transceiver

PL – Programmable Logic

PS – Processing System

QSPI – Quad Serial Peripheral Interface

SoC – System on Chip

USB OTG – Universal Serial Bus On The Go

Executive summary

This report defines the technical specification for the hardware components of the AXIOM system architecture, with the goal to provide the guidelines to design the hardware layer for the multi-core, multi-board, heterogeneous system that has been envisioned by the AXIOM partners in order to meet the expectations of future Smart Cyber-Physical Systems (Smart CPS).

The purpose of this document is to gather the outcomes of the activities performed by all the partners of the AXIOM Consortium in the first nine months of the project's timeframe, and translate them into hardware requirements.

The main subjects that have been addressed and percolated into this hardware specification were the system's architecture and functional requirements.

We define here the AXIOM's structure and its building blocks by taking into account aspects that can lead to a scalable, efficient and easy to program system. Moreover, all the AXIOM industrial partners focused on the need to outline a 'production oriented' specification, keeping in mind the need to establish a roadmap for the system's hardware, in order to track the technology enhancement that is expected within the project's timeframe.

A great contribution to this document came from the use case scenarios definition and the analysis of exploitation opportunities, comparing the AXIOM concept against possible exploitation paths and the use case scenarios that have been built to evaluate the board. This information has been translated into the definition of the AXIOM architecture, its external interfaces and its functional requirements.

A roadmap defines also the next possible evolution of this architecture. The best possible choices available at the time of actual design will be used.

1 Introduction

1.1 Document structure

This document outlines the requirements for the hardware platform used in the AXIOM project, in order to use the resulting technical specification in the implementation of the actual hardware prototype. Section 2 addresses the main goals of the technical specification as outlined in the executive summary.

1.2 Relation to other deliverables

The AXIOM project, as stated by [1], aims at researching new software/hardware architectures for Smart CPSs to meet the following:

- high computational power
- energy efficiency
- scalability and modularity
- easy programmability

AXIOM enables easy programmability of multi-core multi-board systems through the open-source OmpSs programming model, leveraging a form of Distributed Shared Memory (DSM) across interconnected modules (Figure 1).
The OmpSs will also allow accelerating functions through an FPGA. Modular scalability is enabled by a fast interconnect, which is one of the main goals of AXIOM. Such a high throughput and low latency interconnect ARM-based modular boards are going to provide the capabilities for interfacing the physical world and be used in key scenarios such as Smart Video-Surveillance and Smart Living/Home (Domotics).

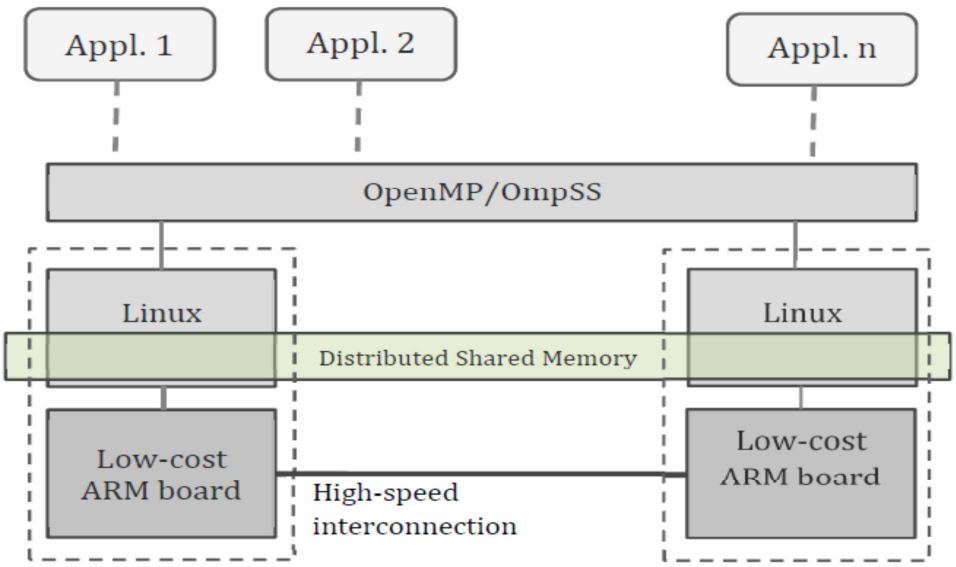


Figure 1 - AXIOM support for OmpSs

This deliverable collects the foreseen requirements applicable to the underlying hardware platform, concerning: performance, functionalities, external interface, resources.
Many of the requirements gathered within this document were directly derived from AXIOM's proposal because they're tightly coupled with the AXIOM concept itself. Other requirements are the outcome of the interaction between WP6 partners, as outline in Task T6.1.
It is worth to mention that most of the external interface requirements were outlined from the outcomes of WP2 and WP3, which focused on the project's exploitation path use case scenarios definition. From the architectural performance and functional perspectives, the main contributions came from WP4, WP5 and WP7.

1.3 Tasks involved in this deliverable

This document is the output of the Task T6.1, and actually involved all the partners within the Consortium, but in particular BSC, FORTH, VIMAR and UNISI, besides SECO as WP-leader, in order to assess architectural and functional requirements for the hardware platform, based on simulation, prototyping and evaluation of the solutions currently available on the market; as already pointed out application scenarios development concurred to this deliverable as well.

2 Hardware technical specification

The first draft of the hardware technical specification was developed wrapping up all the discussions and the outcomes from previous activities, starting from the kick-off meeting, and was presented on 17th September 2015 during the face-to-face meeting in Crete. This final version reflects changes and improvements based on the feedback of the review from the partners.

2.1 Architecture definition

In order to implement the concept described by [1] and improve exploitation possibilities, the hardware architecture has been evolved up to the structure shown in Figure 2.

From the hardware perspective, one of the most relevant topics in the AXIOM system is the interconnect (referred here as the AXIOM-link interconnect) between each system's node. The AXIOM-link interconnects (cf. Section 2.4) must provide, as foreseen in [1], cheap connectors with high-throughput capabilities.

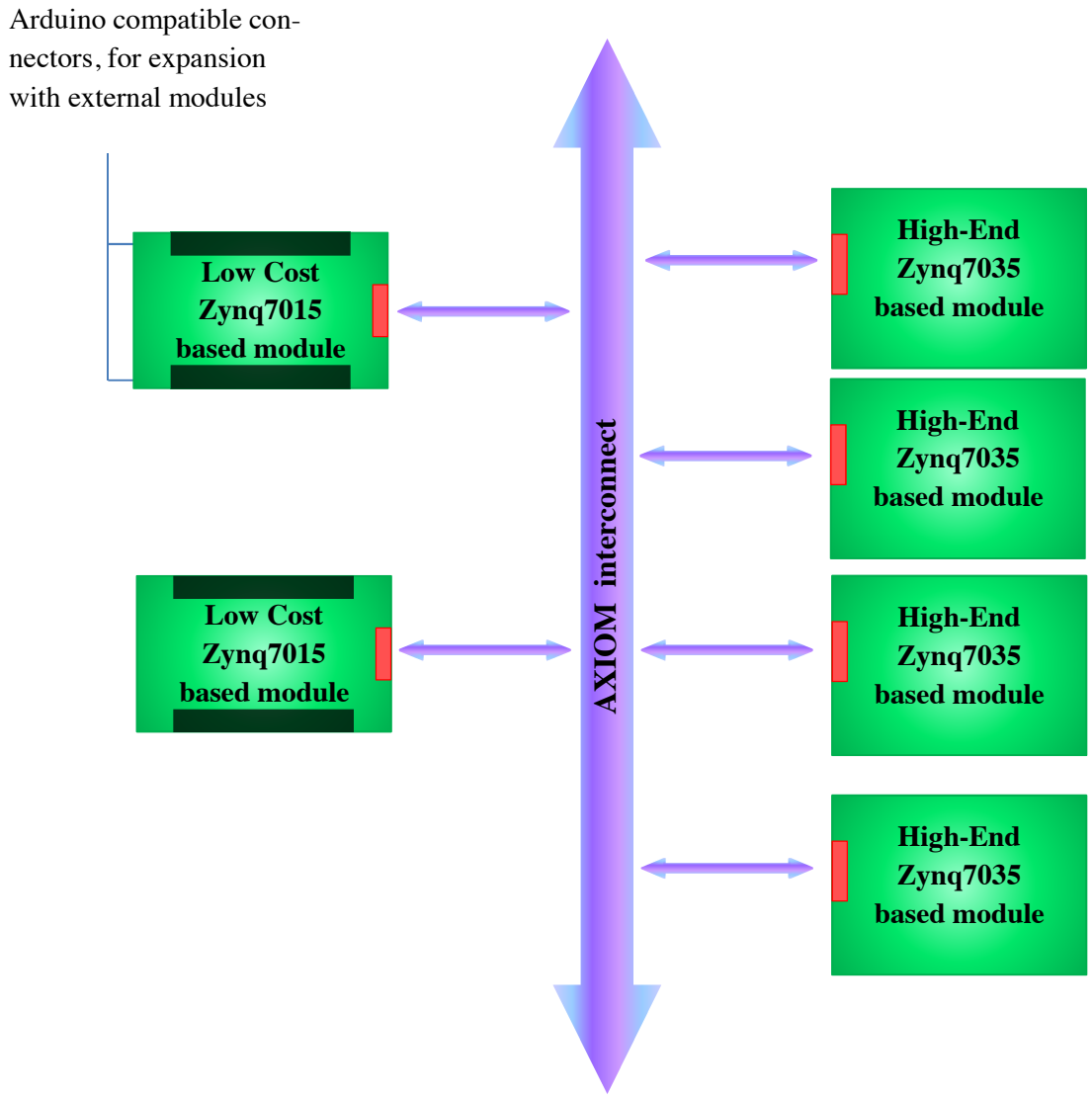


Figure 2 - A scenario deploying two different flavors of the AXIOM board

The overall architecture outlined in Figure 2, points out that the system's prototype is based on two different modules based on Zynq-7000 SoC.

As agreed with the partners, after careful review of several available options, the main choice regards the Zynq-7000 SoC as principal chip, as it provides a good balance between flexibility, computational power, efficiency and cost. In particular, we selected the 7015 and 7035 due to the availability of enough higher speed transceivers (4 for the 7015 and 8 for the 7035).

Therefore, the Consortium decided to focus on two flavors of the AXIOM board: a high-end board based on the XC7Z7035-based module, which will sustain computational tasks (hereafter referred as "**AXIOM-35**") and a low-end board based on the XC7Z7015-based module (hereafter referred as "**AXIOM-15**"), which will interface the external world through sensors/actuators providing popular and easy-to-use interconnections such as the Arduino compatible connector. Please note that the actual AXIOM interconnects is not defined here, as it is under exploration, but in this document we are defining the physical elements to support such interconnect.

Beyond the prototype implementation, the selected architecture may allow us to build modules based on eventually different SoCs, as long as AXIOM-link interconnects and software stack compatibilities are guaranteed. So hybrid implementations and technology tracking are consistently taken into account. A possible roadmap for AXIOM board architecture is outlined in Figure 3.

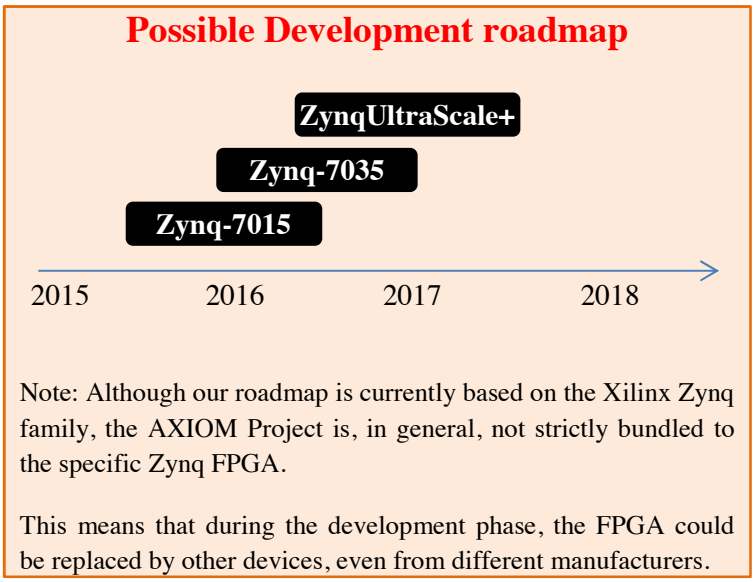


Figure 3 - AXIOM roadmap

Important note: this specification will be updated during the following months with regards to the listed and other types of connectors, based on the actual physical design drafts performed by SECO.

2.2 Functional requirements

This section aims at defining functional requirements for the AXIOM system components outlined in section 2.1. In order to define a mandatory requirement, the verb 'shall' will be used, while the verb 'should' will denote guidelines or recommendations.

2.2.1 SoC

The AXIOM system's prototype will be based on Zynq-7000 SoC family.

The AXIOM-35 board shall integrate the following Zynq-7000 family P/N: XC7Z7035.

The AXIOM-15 board shall integrate the following Zynq-7000 family P/N: XC7Z7015.

2.2.2 System memory

The AXIOM-35 shall integrate 1GB DDR3L for PS (Processing System) and should integrate up to 1GB for PL (Programmable Logic).

The AXIOM-15 shall integrate at least 1GB DDR3L for PS.

2.2.3 Mass storage

The AXIOM-35 shall integrate a uSD slot and should integrate an optional eMMC (4GB minimum).

The AXIOM-15 shall integrate a uSD slot.

Both modules should integrate an optional QSPI EEPROM to provide boot flexibility.

2.2.4 Boot devices

The Zynq-7000 has wide boot device configuration options [2]; the device from which the Zynq's PS has to load the bootloader, shall be selectable through jumpers, in order to provide enough boot flexibility.

2.2.5 Video outputs

Both the AXIOM-15 and AXIOM-35 boards shall integrate HDMI video output.
Single channel 24 bit LVDS I/F, suitable to interface an LCD with touch panel, should be provided as an option on both modules.

2.2.6 USB ports

Both the AXIOM-15 and AXIOM-35 shall provide one USB host interface integrating an USB A connector and optionally an USB OTG interface through a USB micro AB one.

2.2.7 JTAG I/F

Both modules, shall route the Zynq's JTAG interfaces externally. Figure 4 shows JTAG chain implemented within Zynq devices: the suggested implementation is cascaded JTAG mode, as described by [3].
Independent JTAG modes should be implemented as an option. If convenient for board layout, suggested implementation is ARM20 header connector.

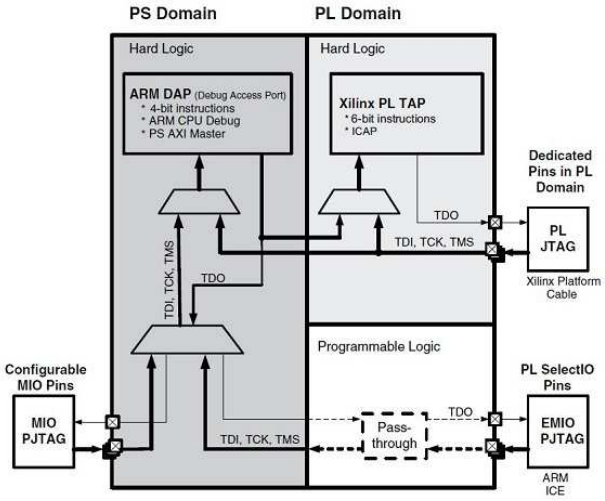


Figure 4 - JTAG options on Zynq-7000

The PL's JTAG port should be interfaced by means of an integrated JTAG programmer compatible with Xilinx's development tools in order to avoid the needs for an external JTAG programmer.

2.2.8 Debug serial port

Both modules shall allow users to access the debug console for the PS. A convenient implementation should integrate an USB to UART bridge to interface the SoC's debug serial port, so it can be externally available as a dedicated mini-B USB connector. If board's layout constrains for module 'B' do not allow an USB to UART bridge, a CMOS level interconnect shall be available through a header connector; the possibility to route a serial debug console through JTAG I/F should be considered as well.

2.2.9 Connectivity

Both modules shall implement the "AXIOM-link interconnect" as primary interface between system's nodes, and Gigabit Ethernet ports will be used as management and general purpose external I/Fs.
According to [4] and [5] the AXIOM-35 should route externally 8 GTX transceiver TX and RX pairs while AXIOM-15 should route externally 4 GPT transceiver TX and RX pairs.
AXIOM-15 should implement WiFi/Bluetooth connectivity in order to allow AXIOM systems (Smart CPS) to interface easily also to wireless devices and sensors such as Internet-of-Things (IoT) devices.

2.2.10 Arduino compatible connector

The AXIOM-15 shall implement Arduino Uno pinout in order to interface Arduino shields, which allows system's expandability to the physical worlds and provides a convenient way to connect AXIOM to a plenty of sensors and actuators already available in the market.

2.2.11 Video decoding capabilities

The AXIOM-35 shall provide H264 or JPEG/JPEG2000 decoding up to 4K resolution @ 30 fps.

2.2.12 Audio

The AXIOM-15 shall provide I2S audio interface, routed to a header connector.

2.2.13 Power-up and reset

Modules shall implement power up and reset buttons and 3 LEDs: a green one to show that board's power up, a red one showing that PL has been successfully programmed and an optional user configurable one, if compatible with mechanical constraints. Both modules should automatically boot once powered up.

2.2.14 Power supply

Both modules shall be supplied through 12 V_{DC} power supply; power jack connector is the suggested implementation for AXIOM-15.

The possibility to power AXIOM-15 from the USB device receptacles should be evaluated in the implementation phase. This would provide a convenient programming setup with reduced wiring; functional or performance limitations which may be required to keep the overall power consumption below 2.5W, would be tolerated in this specific operating condition.

2.2.15 Additional external interfaces

The AXIOM-35 should optionally provide, if compatible with the other requirements, extra GPIO pins routed to a convenient header connector. Suggested electrical level is CMOS 3,3V; If possible, those GPIOs should be configurable to I2C and/or SPI bus.

2.2.16 Sensors

The AXIOM-15 shall integrate the following sensors:

- 3-axis accelerometer
- 3-axis magnetometer
- 3-axis gyroscope

In order to connect further external sensors to the AXIOM-15 board, a dedicated I2C interface should be routed to a convenient connector.

2.2.17 Camera input

The AXIOM-15 should provide a camera input; MIPI CSI should be considered as the preferred implementation.

2.2.18 Operating temperature range

Operating range for both modules shall be at least 0°C – 40°C.

2.2.19 Mechanical dimensions

No specific constraints are set for AXIOM-35, while the suggested dimensions for AXIOM-15 are 56mm x 88.6mm. A tentative layout is shown in pictures below:

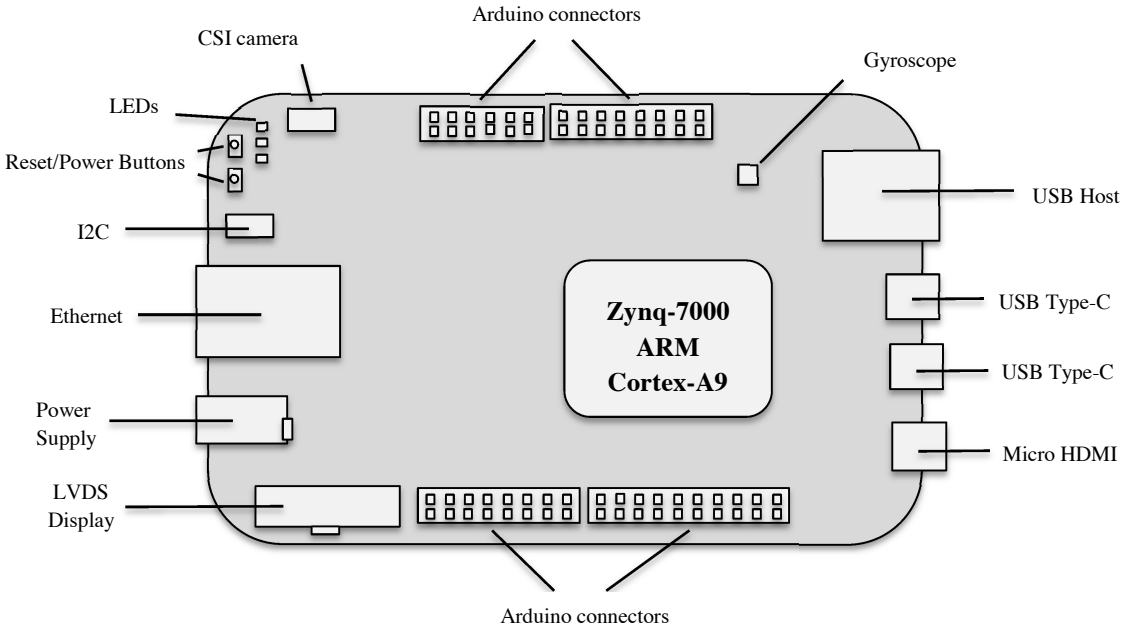


Figure 5 – Tentative layout for AXIOM-15 board (top layer)

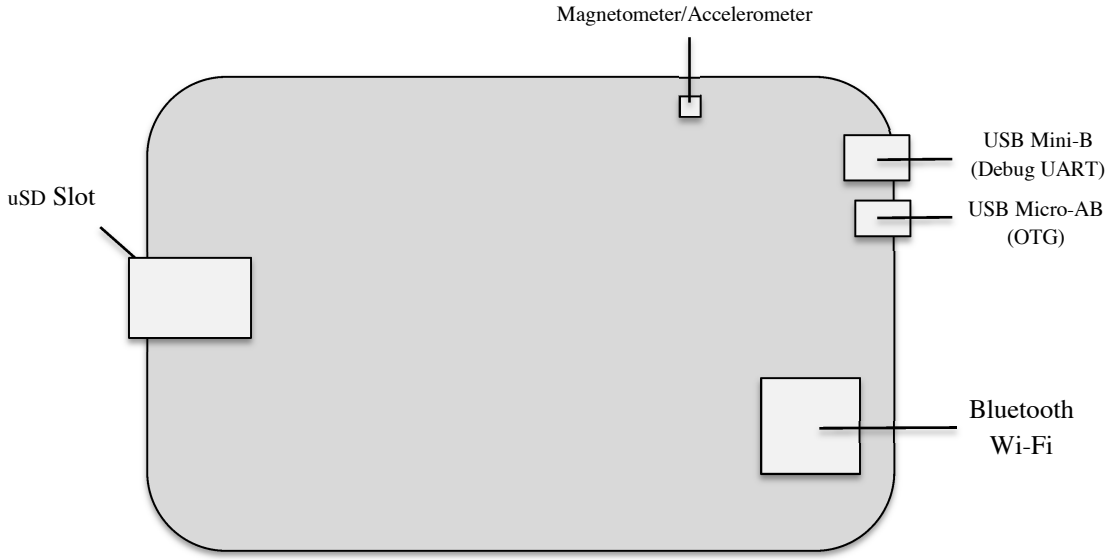


Figura 6 - Tentative layout for AXIOM-15 board (bottom layer)

2.3 AXIOM-link interconnect

AXIOM-link interconnect has to provide a flexible, low cost and high throughput link between multiple AXIOM-15 and AXIOM-35 boards in order to arrange small clusters. To accomplish this goal, cables used in consumer products have been identified as the better option.

From our analysis, the best tradeoff between cost, performance and ease of use has been recognized in type-C cables and receptacles.

AXIOM-15 board shall integrate 2 USB Type-C receptacles

AXIOM-35 board shall integrate 4 USB Type-C receptacles

USB Type-C receptacle, shown in Figure 7, shall implement the pin assignment outlined in Table 1

.

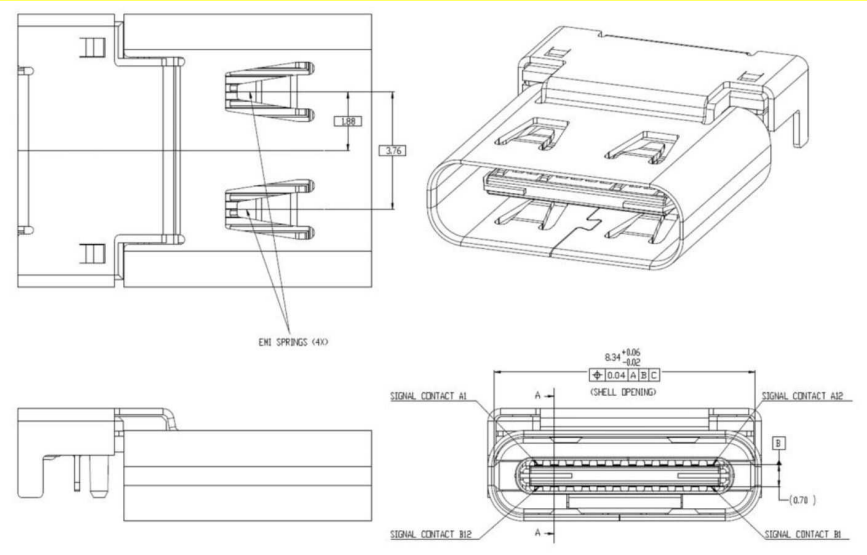


Figure 7 – Type-C USB connector

AXIOM-15 and AXIOM-35 shall integrate the circuitry to implement TX/RX pair swap, which results from USB Type-C cable because it has no mechanical key and can be inserted either right-side-up or upside-down position. TX/RX multiplexing logic should be compatible with the USB specification in order to guarantee proper differential pair routing.

AXIOM boards shall address all the applicable clocking requirements for GTP/GTX transceivers provided by the Zynq SoC.

Table 1 - AXIOM-link interconnect over USB type -C connector

Pin	Name	Notes	Pin	Name	Notes
A1	GND		B12	GND	
A2	SSTXp1	TX differential pair #1, positive	B11	SSRXp1	RX differential pair #1, positive
A3	SSTXn1	TX differential pair #1, negative	B10	SSRXn1	RX differential pair #1, negative
A4	VBUS	Bus power – optionally connected	B9	VBUS	Bus power – optionally connected
A5	CC1	Configuration channel	B8	SBU2	Sideband Use
A6	Dp1	USB 2.0 differential pair, position 1, positive – optionally connected	B7	Dn2	USB 2.0 differential pair, position 2, negative – optionally connected
A7	Dn1	USB 2.0 differential pair, position 1, negative – optionally connected	B6	Dp2	USB 2.0 differential pair, position 2, positive – optionally connected
A8	SBU1	Sideband Use	B5	CC2	Configuration channel
A9	VBUS	Bus power – optionally connected	B4	VBUS	Bus power – optionally connected
A10	SSRXn2	RX differential pair #2, negative	B3	SSTXn2	TX differential pair #2, negative
A11	SSRXp2	RX differential pair #2, positive	B2	SSTXp2	TX differential pair #2, positive
A12	GND		B1	GND	

The AXIOM-link interconnect provides some optionally connected pins; those pins are not required when using the USB Type-C connector to implement AXIOM link, they should be optionally connected when providing functionalities compliant with [6] (USB Type-C cable specification). Although it is beyond the goal of this specification, the intended implementation of AXIOM-link interconnect over USB Type-C connector is not in contrast with the usage of AXIOM-link interconnect as a standard USB 3.1 link.
As specified in [6], AXIOM boards shall provide a differential characteristic impedance of 90Ω ± 10Ω on SSTX and SSRX pairs and D+/D- pair as well; moreover [6] outlines SE and differential voltage range allowed for AXIOM-link interconnect.

Table 2 - AXIOM-link interconnect DC specifications

AXIOM-link interconnect – DC specifications				
DC parameter	**Min**	**Typ**	**Max**	**Units**
Differential peak-to-peak voltage	150	-	2000	mV
Single ended voltage	-	-	1100	mV
Characteristic trace impedance for SSTX, SSRX and D+/D- pairs	-	90	-	Ω

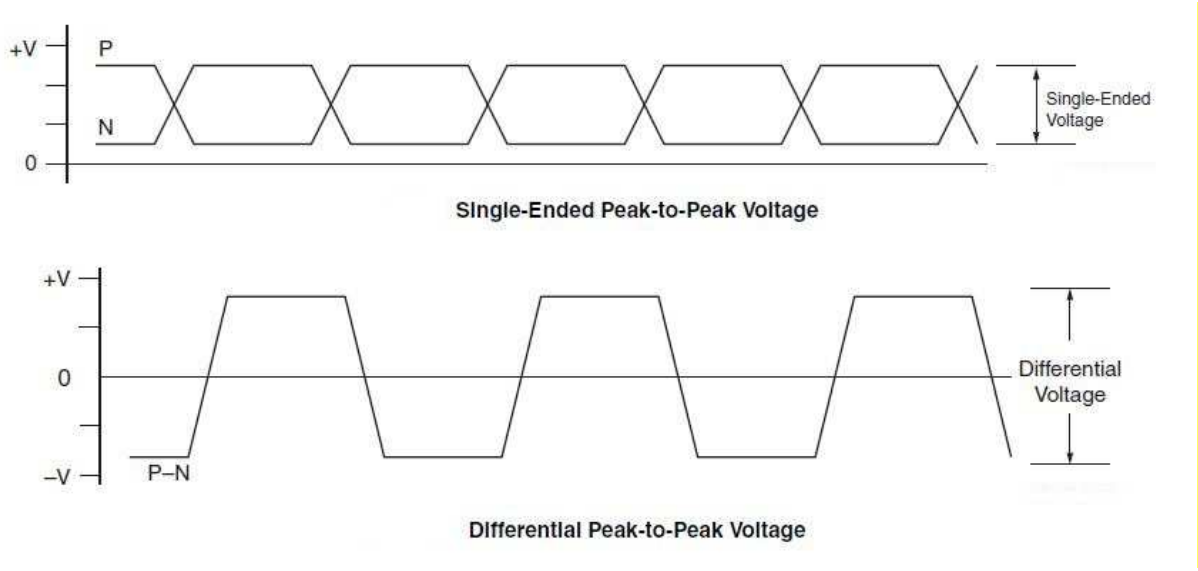
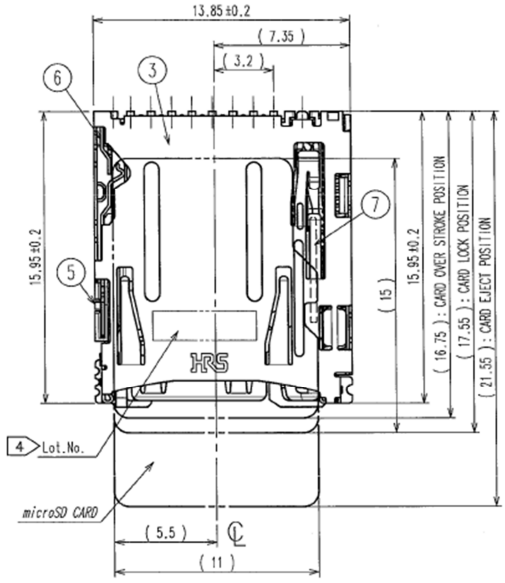


Figure 8 – Single Ended and Differential voltage

2.4 System interface

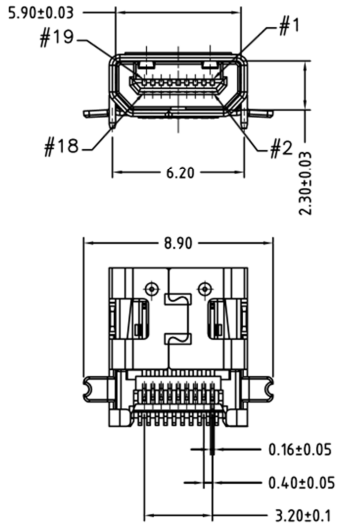
2.4.1 AXIOM-15 and AXIOM-35 external interfaces/connectors

This section defines the electrical requirements outlined in section 2.2 for the AXIOM-15 and AXIOM-35, in terms of P/N for connectors, pinout and electrical levels, if needed.

<table>
<tr><th colspan="3">uSD</th></tr>
<tr><th colspan="2">Manufacturer: HIROSE</th><th>P/N: DM3AT-SF-PEJM5</th></tr>
<tr><th>PIN #</th><th>NET</th><td rowspan="10"> 

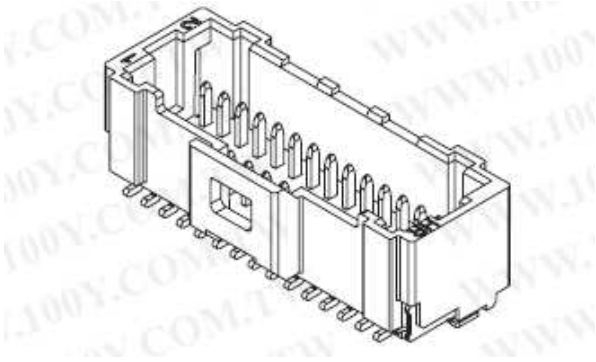
Series image –reference only</td></tr>
<tr><td>1</td><td>SDIO_DAT2</td></tr>
<tr><td>2</td><td>SDIO_DAT3</td></tr>
<tr><td>3</td><td>SDIO_CMD</td></tr>
<tr><td>4</td><td>+3,3 V</td></tr>
<tr><td>5</td><td>SDIO_CLK</td></tr>
<tr><td>6</td><td>GND</td></tr>
<tr><td>7</td><td>SDIO_DAT0</td></tr>
<tr><td>8</td><td>SDIO_DAT1</td></tr>
<tr><td>9</td><td>SDIO_CD</td></tr>
</table>

Micro HDMI			
Manufacturer: FCI			**P/N: 10118241-001RLF**
PIN #	**NET**	**NOTE**	
1	TMDS_LANE2+		
2	GND		
3	TMDS_LANE2-		
4	TMDS_LANE1+		
5	GND		
6	TMDS_LANE1-		
7	TMDS_LANE0+		
8	GND		
9	TMDS_LANE0-		
10	TMDS_CLK+		
11	GND		
12	TMDS_CLK-		
13	CEC		
14	N.C		
15	SCL		
16	SDA		
17	GND		
18	+5V		
19	HPD		



Series image –reference only

LVDS (optional)			
Manufacturer: J-TECH			P/N: A1014WVA-S-2x15P
PIN #	**NET**	**NOTES**	
1	+5V		
2	+5V		
3	+3,3V		
4	+3,3V		
5	LVDS_TX0+		
6	LVDS_TX1+		
7	LVDS_TX0-		
8	LVDS_TX1-		
9	GND		
10	GND		
11	LVDS_TX2+		
12	LVDS_TX3+		
13	LVDS_TX2-		
14	LVDS_TX3-		
15	GND		
16	GND		
17	LVDS_CLK+		
18	BL_ENA	Backlight enable 3,3V CMOS	
19	LVDS_CLK-		
20	DIG_ON	Panel enable 3,3V CMOS	
21	GND		
22	GPIO	3,3V CMOS	
23	BL_CTRL	Backlight dimming (PWM) 3,3V CMOS	
24	I2C_SDA		
25	IRQ#	Internally pulled up to 3,3V	
26	I2C_SCL		
27	TOUCH_RST#		
28	+3,3V		
29	GND		
30	GND		



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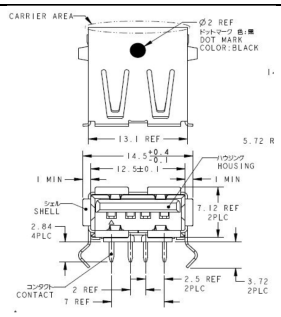
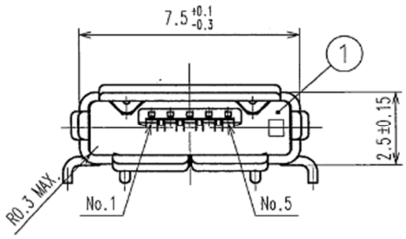
USB type A		
Manufacturer: TYCO ELECTRONICS		**P/N: 1903814**
PIN #	**NET**	
1	VBUS	
2	D-	
3	D+	
4	GND	Series image –reference only

USB OTG micro AB		
Manufacturer: HIROSE		**P/N: ZX62D-AB-5P8**
PIN #	**NET**	
1	VBUS	
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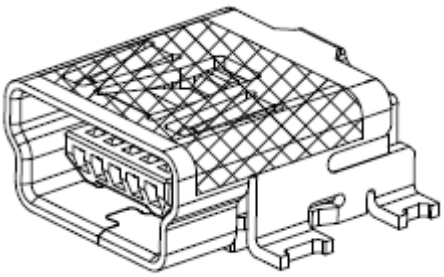
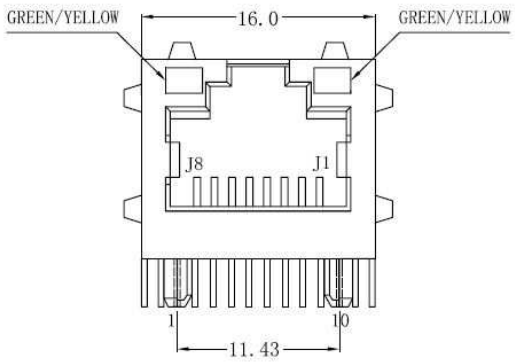
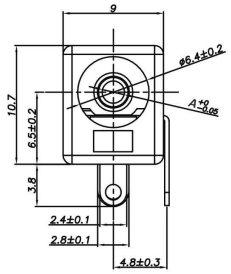
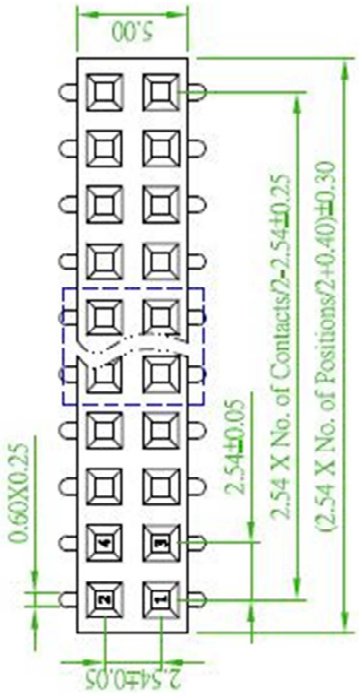
3	D+	
4	ID	
5	GND	Series image –reference only

USB mini B – Debug UART/JTAG BRIDGE		
Manufacturer: TYCO ELECTRONICS		**P/N: 1903814**
PIN #	**NET**	
1	VBUS	
2	D-	
3	D+	
4	ID	
5	GND	Series image –reference only

Gigabit ethernet		
Manufacturer: LINK-PP		**P/N: LPJG16314A4NL**
PIN #	**NET**	 Series image –reference only
1	GND	
2	VREF	
3	MX3+	
4	MX3-	
5	MX2+	
6	MX2-	
7	MX1+	
8	MX1-	
9	MX0+	
10	MX0-	
11	RIGHT_LED_1	
12	RIGHT_LED_2	
13	LEFT_LED_1	
14	LEFT_LED_2	

Power jack		
Manufacturer: WURTH		**P/N:694106301002**
PIN #	**NET**	 Series image –reference only
1	GND	
2	+12V	

Arduino connector			
Manufacturer: AMTEK			**P/N: PS1M71-2XXGBCPR-U**
PIN #	**NET**	**NOTES**	
1	SCL	I2C	
2	SDA	I2C	
3	AREF		
4	GND		
5	SCK	SPI	
6	MISO	SPI	
7	MOSI/PWM	SPI	
8	SS/PWM	SPI	
9	PWM		
10	GPIO		
11	PWM		
12	PWM		
13	PWM		
14	PWM		
15	PWM		
16	GPIO		
17	USART_TX		
18	USART_RX		
19	A0	ANALOG IN	
20	A1	ANALOG IN	
21	A2	ANALOG IN	
22	A3	ANALOG IN	
23	A4	ANALOG IN	
24	A5	ANALOG IN	
25	Vin		
26	GND		
27	GND		
28	5V		
29	3.3V		
30	RESET		



Series image –reference only

3 Confirmation of DoA objectives

As required by the DoA, this deliverable (D6.1) is provided in the form of a formal technical specification that outlines the most relevant architecture details, which have been gathered during the first nine months of the AXIOM project.

PLANNED	DELIVERED
DELIVERABLE:	
Technical specification of AXIOM board	Technical specification outlining: • Architecture definition • Functional requirements • External interface • Mechanical/environmental requirements

4 Conclusion

This document establishes the hardware technical specification for the building blocks of the AXIOM system. The requirement expressed in this specification will be an input for the next tasks scheduled for WP6, which is targeted to hardware implementation of the boards that will be used to build the prototype of the AXIOM system.

References

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2. ds190 Zynq-7000 - Overview

   http://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf

3. ug585 Zynq-7000 – Technical Reference Manual

   http://www.xilinx.com/support/documentation/user_guides/ug585-Zynq-7000-TRM.pdf

4. ds187 Zynq-7000 (Z-7010, Z-7015, Z-7020) – DC and AC Switching Characteristics

   http://www.xilinx.com/support/documentation/data_sheets/ds187-XC7Z010-XC7Z020-Data-Sheet.pdf

5. ds191 Zynq-7000 (Z-7030, Z-7035, Z-7045, Z-7100) – DC and AC Switching Characteristics

   http://www.xilinx.com/support/documentation/data_sheets/ds191-XC7Z030-XC7Z045-data-sheet.pdf

6. Universal Serial Bus Type-C Cable and Connector Specification – Revision 1.1